TYPE GSDA/1
GATED SIGNAL DATA ANALYSER
HANDBOOK

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HANDBOOK FOR GATED SIGNAL DATA ANALYSER TYPE GSDA/1

INTRODUCTION

The GSDA/1 has been designed as a general-purpose instrument for the processing of radar video signals, in order to simplify the investigation of certain aspects of radar performance.

The video pulses of interest must be distinguished from all other video signals by the coincident occurrence of area gate pulses, which would normally be generated by a Type AGG/2 Area Gate Generator.

The GSDA/1 contains circuits which perform the following functions:

(a) **Video signal amplification**: Gain is selected by a switch on the front panel which can be set to x1, x2, x5 or x10. The amplified signal (ungated) is available from a BNC socket, which should be loaded with 75Ω.

(b) **Video signal gating**: After amplification as in (a) above the video signal passes through an electronic switch, which is only closed when area gate pulses occur. The gated video is available from a BNC socket, which should be loaded with 75Ω.

(c) **Generation of "Video + Pedestal" waveform**: This waveform is produced by addition of the incoming gate waveform to the amplified ungated video signal. The peak voltage of the video pulses which are of interest is therefore increased relative to all other video pulses. Pedestal amplitude may be varied by means of a knob on the front panel. The Video + Pedestal waveform is available from a BNC socket, which should be loaded with 75Ω.

(d) **Generation of "Beam Profile" waveform**: This waveform, which appears rather like a histogram when displayed on an oscilloscope, is produced by applying the gated video pulses to a peak detector circuit. The peak detector circuit temporarily stores each peak pulse potential as an analog voltage, which is then sampled by a sample-and-hold circuit immediately after the trailing edge of each gate pulse. The output of the sample-and-hold circuit constitutes the Beam Profile waveform, and is available from a BNC socket which should be loaded with 75Ω.

(e) **Generation of "Regenerated Video" pulses**: A threshold potential may be set by means of an accurately calibrated control on the front panel. Should this threshold potential be exceeded by any incoming video signal within the gated area, a monostable circuit will be triggered. The monostable circuit outputs a 5μs pulse at TTL level, which is available at a BNC socket. The circuit is capable of generating only one pulse per PRI, and the generation (or otherwise) of a pulse is not affected in any way by the setting of the Gain Control Switch.

(f) **Generation of X, Y and Z signals for special oscilloscope display**: When correctly set up, the special oscilloscope display shows all the gated video pulses arranged side by side, with a numeric display of the time of day below them. The X and Y signals should each be loaded with 75Ω; the Z signal is at TTL levels, being at logical 0 (approx. 0V) when it is required to switch the beam off. Also available is a $\overline{Z}$ output signal; this output switches between +15V and −15V w.r.t. ground, being at +15V when it is required to switch the beam off. All four output signals (X, Y, Z, $\overline{Z}$) are available at BNC sockets.

In order to display the time data, it is necessary to supply a time code signal to the GSDA/1. Such a signal may be generated by a Type TCG/1 Time Code Generator & Reader. Connection is by means of a BNC socket.

There are controls on the front panel to allow for adjustment of horizontal shift, horizontal amplitude, character vertical shift, and character vertical amplitude. To simplify adjustment of character size and position, a continuous bright display of the characters may be presented by operation of an appropriate switch.

Once the horizontal amplitude has been set by means of the control mentioned above, this amplitude can be maintained regardless of any change in the width or length of the gated area by means of a circuit which automatically compensates by varying the ramp rate of the X waveform. Should it be required to maintain the ramp rate at a constant value, however, a switch is provided to enable it to be fixed at whatever value it happens to be when the switch is operated. A third position on this switch allows the operator to select a "magnified" video display, in which all returns are superimposed on each other; this facility allows a more detailed inspection of SSR returns to be made.

(g) **Generation of Camera Control signals**: Two relays within the GSDA/1 have their contacts brought out to a 5-way socket. For correct operation, closure of one pair of contacts must hold the camera shutter open, whilst closure of the other pair must cause the film to be advanced to the next frame. Provided a camera having this control facility is employed, series of photographs of, for instance, the XYZ oscilloscope display described in (f) above can be taken automatically. Indicator lights on the front panel show the camera status, and a control switch allows for the taking of either single shots or a continuous series.

(h) **Strike Count**: A circuit counts the Regenerated Video pulses previously described in (e) above. The total obtained represents the strike count, which is passed to a Formatter for subsequent output in serial ASCII form (see (1) below). The counting circuit is reset to zero immediately prior to each new group of returns.

(j) **Measurement of Peak Return Amplitude**: Each output of the peak detector described in (d) above is converted to digital form by a circuit which also behaves as a digital peak detector. After a group of returns has occurred, the output data from this circuit represents the amplitude of the highest pulse in the group. The data is passed to the Formatter for subsequent output in serial ASCII form (see (1) below).

(k) **Measurement of Integrated Return Level**: The data representing individual return amplitudes are summed by a digital integrator. The resultant integrated data may be regarded as a "figure of merit" for the group of returns, since it must theoretically equal the product of the number of returns and their average amplitude. Here it should be noted that the number of returns is not necessarily the same thing as the Strike Count mentioned in (h), because the latter is dependent upon the setting of the threshold potential. In a totally noise-free system, however, it would in theory be possible to set the threshold level virtually to zero, in which case the number of returns would be equal to the Strike Count data.

The integrated data is passed to the Formatter for subsequent output in serial ASCII form (see (1) below).

(1) **Output of data in serial ASCII form**: The data produced as described in (h), (j) and (k) above is all incorporated into a single serial ASCII message. Space characters are inserted in the message between the different data, and leading zeros are converted to space characters. The data can therefore be fed directly to a teleprinter to obtain results immediately in hard copy. In the design of the GSDA/1 it has been assumed that the output of the serial message will be initiated by a signal from the AGG/2, and the data plug wiring has been arranged to facilitate this.

The format of the output data is controlled by a program stored in a plug-in ROM (read-only-memory). By replacing the ROM the format can easily be changed if required.

(m) **Source Selection**: The GSDA/1 has a source selection switch on the front panel, to enable it to be used in conjunction with either of two separate AGG/2s. For convenience, these are referred to as the left AGG/2 and the right AGG/2 (L and R). There are therefore two video inputs, two gate inputs, and two 5-pin data connectors, in each case labelled "L" and "R". When the source selector switch is set to "LEFT" all the "right" inputs are open circuited, and vice versa.

(n) **DC isolation of video signal**: A three-position switch on the front panel enables the selected video input signal to be connected either directly or via a 6.8 μF capacitor, or to be disconnected completely (leaving the input open circuit). Maximum permissible voltage across the capacitor is 100V.

SPECIFICATION

MECHANICAL

The GSDA/1 is housed in a rectangular metal case, with carrying handles at the front. All operational controls are situated on the front panel. All electrical connections are made at the rear. There are two folding legs under the case which enable it to be tilted for easier access to controls if required.

The unit may be withdrawn from the case by undoing four slot-head screws on the front panel. It can then be mounted in a standard 19-inch rack if required.

The connectors at the rear (except for the mains connector) are all mounted on a bracket, which is held in place by a single screw. When this screw is undone the bracket may be swung upwards on hinges to enable the printed circuit boards to be withdrawn.

With one or two minor exceptions, all screws, nuts and washers used in the GSDA/1 are metric sizes, M2, M3, M4 or M5.

Case dimensions (overall):	Height	170 mm.
	Width	495 mm.
	Depth	351 mm.
Front panel:	Height	133 mm.
	Width	483 mm.
	Thickness	3.25 mm.
	Fixing centres	465 x 57.2 mm.
Frame dimensions:	Height	133 mm.
	Width	445 mm.
	Overall depth measured from rear of front panel: 300 mm.	
Weight:	With case:	15 Kgm.
	Without case:	10.5 Kgm.

ELECTRICAL

Signal Inputs	R_{in}	Recommended signal amplitude	Rating	
			$V_{min.}$	$V_{max.}$
L & R Video	75Ω when selected. ∞ when not selected.	0 to +5V	−17V	+17V
L & R Gate	1KΩ when selected. ∞ when not selected.	+2V	−50V	+50V
Time	10KΩ	±1V	−50V	+50V
L & R Data control inputs – "Reset" (pin 1) and "Begin" (pin 4)	620Ω to +5V when selected. ∞ when not selected.	TTL levels	−0.5V	+5.25V

Signal Outputs	R_{out}	Recommended Load	Recommended Max. Signal Excursion	
			Loaded	Unloaded
Video	75Ω	75Ω	− 5V to + 5V	−10V to +10V
Gated Video	75Ω	75Ω	− 5V to + 5V	−10V to +10V
Video + Pedestal	75Ω	75Ω	− 5V to + 5V	−10V to +10V
Beam Profile	75Ω	75Ω	0 to + 5V	0 to +10V
X	75Ω	75Ω	− 5V to + 5V	−10V to +10V
Y	75Ω	75Ω	− 5V to + 5V	−10V to +10V
Z	TTL	TTL	0 to + 3V	0 to + 3V
$\overline{Z}$	1KΩ	∞	−15V to +15V	−15V to +15V

FRONT PANEL CONTROLS & INDICATORS

Mains Switch & Indicator

The main switch interrupts the mains supply to the transformer in the Power Supply Unit. The indicator is lit by the unregulated d.c. supply of approximately +11V from the Power Supply Unit.

Source Selector Switch

This is associated with the Video, Gate, and Data connectors at the rear of the GSDA/1; a "left" and a "right" connector are fitted for each of these functions. The Source Selector Switch has three positions, the effect of each position being:

"LEFT": Only the "left" Video, Gate and Data connectors are functional, the "right" connectors being open-circuited.

"RIGHT": Only the "right" Video, Gate and Data connectors are functional, the "left" connectors being open-circuited.

"L.IN/R.OUT": The "right" Video, Gate and Data connectors are functional as though the switch were in the "right" position, but additionally, the "left" data connector can now be used to receive data from a subsequent device, for retransmission via the "right" data connector.

AC/DC Switch

This switch has three positions, which have the following effects:

"DC": Video signals from the selected input are passed directly to the Video Gain switch. Input impedance to selected video is thus 75Ω.

"AC": Video signals from the selected input are passed via a 6.8μF capacitor to the Video Gain switch. Input impedance is thus 75Ω in series with 6.8μF, and video frequencies below about 300 Hz will be rejected.

"DISCONNECTED": The switch presents an open circuit to the selected video signal.

Video Gain

This switch has four positions labelled "x1", "x2", "x5" and "x10". The switch is a 75Ω attenuator which introduces attenuation of 20dB, 14dB, 6dB or 0dB in each of the respective positions. The setting of the switch affects the level of the video signal fed to all parts of the GSDA/1 for analysis EXCEPT the strike counting circuit, which is always fed with unattenuated video.

Strike Count Threshold Potential

This is a precision potentiometer which allows the threshold potential to be set accurately to any level between 0V and +10V (although normally it would not be set to a value greater than +5V). The strike count threshold potential is the potential which the video signal must exceed during a gate period in order for a target "strike" to be recognised. Each time a strike is recognised the strike count data for that sweep is incremented by one, and a 5 μs pulse is output at the "Regenerated Video" socket.

Pedestal Amplitude

This control varies the height of the pedestal component of the "Video + Pedestal" output signal. Note that pedestal amplitude is not increased by actually raising the video base line during the pedestal, but rather by lowering it when the pedestal is not present. The base line is thus always at approximately zero volts during the pedestal period, regardless of the setting of the Pedestal Amplitude control.

Camera Status Indicators

"Shutter Open": This indicator lights whenever the shutter control relay contacts are closed.

"Film Advance": This indicator lights whenever the film advance relay contacts are closed.

"Ready": This indicator lights when the camera control mode switch is in the "Standby" position and the camera control circuit is ready to start a new sequence.

Camera Control Mode Switch

This switch has two stable positions, labelled "Repetitive" and "Standby", and a third (non-locking) position labelled "Single Shot". The camera control circuit in the GSDA/1 causes the shutter control relay and the film advance relay to operate sequentially, holding the camera shutter open whilst the wanted video display is produced on the oscilloscope, and then closing it and advancing the film to the next frame. The effects of the different switch positions are as follows:

"Repetitive": The above sequence of operations takes place continuously, synchronised with the occurrence of area gate pulses. Thus a photograph will be taken with each aerial revolution.

"Standby": The control circuit will complete its current cycle in an orderly fashion and then halt with the film advanced ready for the next shot, but with the shutter closed. When it has halted, the "Ready" indicator will light up.

"Single Shot": When the switch is depressed to this position the shutter relay contacts immediately close, opening the camera shutter. After the occurrence of the next area gate pulses the shutter contacts open and the film advance contacts close, and then the sequence halts as before with the "Ready" indicator on.

Horizontal Signal Shift

This control varies the d.c. bias on the "X" output signal, and can thus be used to shift the "XYZ" display to the left or right as required.

Horizontal Signal Amplitude

This control varies the amplitude of the "X" output signal, and can thus be used to adjust the width of the "XYZ" display.

Horizontal Signal Mode Switch

This switch controls that part of the "X" signal responsible for horizontal deflection during the video pulse display section of the "XYZ" output. It has three positions, which have the following effects::

"Fix Amplitude": The overall horizontal amplitude of the display is maintained approximately constant regardless of the size or shape of the gated area. In this mode deflection speed will vary if the area gate size is changed.

"Fix Ramp Rate": The deflection speed is fixed at whatever value applied when the switch was operated. In this mode the horizontal amplitude will vary if the gate size is changed. (**NOTE**: Before switching to this mode the "Fix Amplitude" mode should first be selected for at least one aerial revolution).

"Magnify": A conventional sawtooth waveform is generated during each area gate pulse. Horizontal amplitude is proportional to gate pulse length.

Character Display Vertical Shift

This control may be used to vary the position of the characters relative to the video pulses in the "XYZ" display.

Character Display Vertical Amplitude

This control may be used to vary the height of the characters in the "XYZ" display, and should be adjusted to give optimum legibility.

Character Display Mode Switch

This switch has two positions, labelled "Normal" and "Continuous". It should normally be set to the former position, which will result in the character display being painted on the oscilloscope once per aerial revolution, immediately after the painting of the video pulses.

Switching to the "Continuous" position causes a continuous flicker-free display of the characters which may be useful for setting-up or test purposes. Note that when in the "Continuous" mode the data displayed by the characters is not automatically updated but remains constant.

SETTING-UP PROCEDURE

Essential Inputs:

An area gate signal and an associated video signal are essential for any normal use of the GSDA/1, except when it is being used solely as a video amplifier. The peak video level should not exceed 5V. The video and gate signals should be connected to either the "left" or the "right" input sockets. If two independent video signals, determined by two gate signals, are to be analysed, use will have to be made of both the "left" and the "right" socket. The left or right input (as appropriate) should then be selected by means of the selector switch on the front panel.

Other Connections:

If the analysed data is to be logged it will be necessary to make a data connection to the AGG/2, using the left or right data socket as appropriate. If use is to be made of the XYZ oscilloscope display and photographic records made, it will be necessary to provide a time code signal from the TCG/1 Time Code Generator.

Setting of Controls:

1. Source selection: select either "left" or "right" as appropriate, and either "DC" or "AC" as appropriate (use AC mode if there is a DC offset potential superimposed on the incoming video signal).

2. Gain: if incoming video signal amplitude is in excess of 2.5V set gain to "x1". If amplitude is less than 2.5V set gain to "x2". If less than 1V set gain to "x5", or if less than 0.5V set gain to "x10".

3. Strike count threshold level: the setting of this control represents the potential which the incoming video signal must exceed during the gate period in order to be regarded as a "strike". Set the control to a value equal to half the expected peak amplitude.

4. If the GSDA/1 is to be used to log data on aircraft returns, and the data link (5-pin connector) to the AGG/2 is therefore fitted, use the AGG/2 to track an aircraft and feed the AGG/2 data output to a printer. The printer should now print time, status (possibly a space character), range, and bearing, all of which are generated within the AGG/2, followed by the data from the GSDA/1, which consists of strike count, peak amplitude, and integrated return level figures. The peak level figures, when divided by the gain control setting, should represent the video peak amplitude as a percentage of 5V.

5. If the XYZ display is to be used, connect the X, Y, and Z or $\overline{Z}$ (as appropriate) signals to the oscilloscope and adopt the following procedure:

(a) Horizontal signal – set SHIFT to 12 o'clock position, AMPLITUDE to maximum counterclockwise position, and mode switch to "FIX AMPLITUDE".

(b) Character display – set VERTICAL SHIFT to 12 o'clock position, VERTICAL AMPLITUDE to maximum counterclockwise position, and mode switch to "NORMAL".

(c) Disconnect X input to oscilloscope and use oscilloscope X shift control to move the spot to the centre of the tube.

(d) Reconnect X input to oscilloscope and, if necessary, re-centre the spot by means of the Horizontal Signal Shift control on the GSDA/1.

(e) Turn the GSDA/1 Horizontal Signal Amplitude control clockwise until the spot moves to the left-hand edge of the tube.

(f) Turn down the oscilloscope brightness until the stationary spot is barely discernible.

(g) Observe the oscilloscope display carefully: when area gating occurs the spot should traverse the tube from left to right, painting the individual video pulses as vertical deflections. It should then paint a short horizontal line beneath the first, then return to its waiting position at the left-hand edge of the tube. Observe this pattern of behaviour several times, then make any small adjustments to the horizontal shift and amplitude controls which may be necessary to obtain a satisfactorily centred display of reasonable width.

(h) Continue to observe the display and adjust the Y gain of the oscilloscope in order to obtain the best video pulse display. If necessary, the picture may be moved downwards by means of the oscilloscope Y shift control, but ensure that a margin of about 1 cm. is left between the base line of the video pulse display and the bottom edge of the display area. Note carefully the level of the base line.

(i) Switch the GSDA/1 Character Display mode to "CONTINUOUS" and turn the Vertical Amplitude control clockwise. The character display will now be painted on the oscilloscope tube. Adjust the Character Vertical Shift and Vertical Amplitude controls as necessary to give a legible character display just beneath the level of the base line of the video pulse display.

(j) Switch the character display mode back to "NORMAL" and turn down the oscilloscope brightness until the stationary spot disappears.

(k) The XYZ display is now correctly set up to display the "beam profile" effect (i.e. pulses standing side-by-side). The GSDA/1 will automatically compensate for any change in the length or width of the gated area by changing the speed with which the spot traverses the tube, thus maintaining an approximately constant horizontal display amplitude. Note, however, that this compensation will not come into effect until after the first paint at the new gate size.

(l) If, having set up the display in the manner described, it is considered necessary to maintain a constant value of horizontal velocity, the Horizontal Display mode switch should now be set to "FIX RAMP RATE".

(m) If it is desired to superimpose all the video pulses (i.e. to get a "sideways view") the Horizontal Display mode switch should be set to "MAGNIFY".

(n) If it is desired to take photographs of the displays using a camera controlled by the GSDA/1, first set the Camera mode switch to "REPETITIVE" and check that the "SHUTTER OPEN" indicator lights up on each aerial revolution well before the occurrence of the area gate pulses.

PRINCIPLES OF OPERATION

This section is intended to be read in conjunction with the System Diagram.

COUNTER AND CONTROL BOARD

This board has five separate functions:

(1) It accepts the area gate signal, which is routed to it from one of the gate input sockets via the source selection switch. It outputs the area gate signal in inverted form to various other boards.

(2) It generates a "busy" signal. This is a pulse to logic 0 which starts on receipt of the leading edge of the first area gate pulse of a group, and does not terminate until about 6 ms after the occurrence of the last pulse of the group. The "busy" signal is output to various other boards.

(3) It compares the level of the selected video signal with an accurate reference voltage from the Strike Count Threshold potentiometer. If the video signal potential exceeds the reference voltage during an area gate period a single 5μs pulse ("regenerated video") is generated. Note that not more than one regenerated video pulse may be generated per area gate pulse. The regenerated video signal is available as an output from the GSDA/1 at TTL level.

(4) It contains a 2-decade BCD counter, which is always set to zero by the leading edge of the "busy" signal and is incremented on the occurrence of each regenerated video pulse. The output of the counter thus represents the Strike Count data, and is routed to the Formatter for eventual output from the GSDA/1 in serial ASCII code.

(5) It contains a camera control circuit which operates the shutter and film advance relays in turn. This circuit is triggered by the "busy" signal, and may operate in either the "repetitive" or "single shot" mode, as selected by the front panel switch. The contacts of the two relays are isolated from all other parts of the circuit, and are brought out to a 5-pin connector at the rear of the GSDA/1. When working in the "repetitive" mode the shutter relay contact closes about one or two seconds before the area gate pulses are due, and remains closed until about one second after their occurrence. It then opens, and about half a second later the film advance contact closes, to open again about two seconds later. The shutter relay then closes and the sequence begins again. In the "single shot" mode the operation is similar, except that after the film advance contact has opened the shutter contact does not close automatically but remains open until the front panel switch is momentarily depressed, when it closes immediately. It then remains closed until about one second after the occurrence of the area gate pulses, as before. Closure of the contacts is indicated by front panel LEDs.

VIDEO ISOLATION BOARD

The Video Isolation Board contains seven output amplifiers, each capable of delivering up to ±5V into a 75Ω load. It also contains an analogue gating circuit and signal-mixing arrangements. The video signal is routed to the input of the Video Isolation Amplifier from an input socket via the source selector switch, AC/DC switch, and the Gain Control switch. The latter introduces attenuation of 20dB, 14dB, 6dB or 0dB, depending upon its setting. The overall gain of the Video Isolation Amplifier from its input to any one of its outputs at which the video signal appears is 20dB when the output is loaded with 75Ω, or 26dB when not loaded.

The video signal first passes through an inverting amplifier, which has a gain of 10dB. The output of this amplifier is used for three purposes, viz:–

(a) It is fed directly to an inverting output amplifier, whose 75Ω output is routed to the "video" socket at the rear of the GSDA/1.

(b) It is mixed with the pedestal signal (which is produced by passing an inverted area gate signal through the Pedestal Amplitude control potentiometer) and then fed to an inverting output amplifier. The output of this amplifier is routed to the "Video + Pedestal" socket.

(c) It is fed to an analogue gating circuit, which only allows the signal to pass during area gate pulses.

The output of the gating circuit in its turn serves three purposes:

(d) It is fed to an inverting output amplifier whose output is routed to the "Gated Video" socket.

(e) It is fed to another inverting output amplifier whose output is routed to the Video Measurement Board.

(f) It is mixed with YCH and YOS signals (which come from the Character Generator Board via the "Character Vertical Amplitude" and "Character Vertical Shift" control potentiometers) and then fed through an inverting output amplifier to the "Y" socket.

The Video Isolation Amplifier also contains non-inverting unity-gain output amplifiers for the "X" signal from the Interrupted Ramp Generator, and for the "Beam Profile" signal from the Video Measurement Board.

VIDEO MEASUREMENT BOARD

Gated Video from the Video Isolation Amplifier is fed to the Video Measurement Board where a peak detector circuit temporarily stores in analogue form a voltage representing the highest video potential occurring during each area gate pulse. After termination of each area gate pulse the stored voltage is transferred to a sample-and-hold circuit, whose output is the "Beam Profile" signal. The peak detector capacitor holding the stored voltage is then discharged at a constant rate, and a crystal-controlled pulse generator is enabled during the discharge period. The number of pulses generated depends upon the time taken to discharge the capacitor, and is thus proportional to the voltage stored. The pulses are counted by a four-stage BCD counter (which is initially set to zero by the leading edge of the "busy" signal), and the total count achieved represents the Integrated Level data, which is routed to the Formatter Board for eventual output in serial ASCII code. The pulses are also fed to a special counting circuit which behaves as a digital "peak detector" and outputs a 2-decade BCD number representing the highest number of pulses detected in any one burst. This "peak amplitude" data is also routed to the Formatter Board for eventual output in serial ASCII code.

TIME DECODER BOARD

The Time Decoder Board receives time code signals, which are in serial bi-phase code and originate from a TGG/1 Time Code Generator. The serial signal is decoded and fed into a shift register. It is then transferred in parallel form to a parallel output register, whence it is routed to the Character Generator Board. The "flag" input to the Time Decoder is used to inhibit the transfer from the shift register whilst the Character Generator is actively making use of the time data.

CHARACTER GENERATOR BOARD

The main function of the Character Generator Board is to generate, at the appropriate time, the X, Y and Z waveforms necessary to cause an oscilloscope to display the time data which is being output by the Time Decoder. The X and Y waveforms (known as "XCH" and "YCH") consist of combinations of steady potentials and positive- and negative-going ramps, whilst the Z waveform consists of rectangular pulses which are intended to switch the oscilloscope beam on.

Since it is also necessary to switch the oscilloscope beam on during area gate pulses in order to achieve a satisfactory "XYZ" display, inverted area gate pulses from the Counter and Control Board are combined with the locally-generated Z signal to form a composite Z signal which is output from the board. $\overline{Z}$ is an inverted version of the Z waveform, being negative-going for "beam on" and having a peak-to-peak amplitude of 30V.

Two further outputs from the board are the offset signals "XOS" and "YOS". These signals are identical, being normally at about +1.75V, but falling to zero during the actual character generation. They are ultimately added in different proportions to the composite X and Y waveforms so as to position the characters correctly on the oscilloscope display.

In order to ensure that the time data does not change during actual character generation, the board sends a logic 1 status signal ("Status (B)") back to the Time Decoder whilst it is operating. This signal inhibits updating of the Time Decoder output data.

The "busy" signal from the Counter and Control Board is fed to the Character Generator, and it is the trailing edge of this signal which actually triggers off the character generating sequence.

INTERRUPTED RAMP GENERATOR

The primary function of this board is to generate the interrupted ramp waveform which controls horizontal beam deflection in the "XYZ" display. The board contains a circuit which automatically adjusts the ramp slope to a value which is inversely proportional to the effective area of the area gate (i.e. length of gate pulses x quantity of gate pulses). This automatic adjustment ensures that the overall amplitude of the X deflection waveform is maintained approximately constant, regardless of area gate size or shape.

If at any time the control switch on the front panel is thrown from the "Fix Amplitude" position to the "Fix Ramp Rate" position, the automatic adjustment facility is inhibited, and the ramp slope remains constant at whatever value obtained at the time when the switch was operated.

If the front panel switch is set to "Magnify" the circuit generates a sawtooth waveform instead of an interrupted ramp, with the effect that the video pulses shown by the XYZ display will be magnified in the X direction, and overlaid on each other instead of standing side-by-side.

The interrupted ramp or sawtooth waveform is mixed with the XCH and XOS signals from the Character Generator and with a d.c. potential from the X Shift Control potentiometer to form the composite X waveform, which is routed from the board via the X amplitude control potentiometer on the front panel to the Video Isolation Board.

FORMATTER BOARD

The Formatter Board receives parallel BCD data representing Peak Amplitude and Integrated Level from the Video Measurement Board, and Strike Count from the Counter and Control Board. On receipt of a transition from logic 1 to logic 0 at its "Begin" input it proceeds to generate an output signal coded in serial ASCII which contains the data, and also various other characters, under the control of a program stored on board in a read-only memory (ROM).

The output and control connections to the Formatter are routed from the 5-pin data connectors via the source selection switch. When the switch is set to "Left" or "Right" an externally-generated "begin" command from the selected socket will cause the serial ASCII signal to be transmitted back to the source of the command. When the switch is set to the "L.IN/R.OUT" position the source of the command must be connected via the "R" socket, and this is where the ASCII output will be routed, but when the output sequence is complete the "flag" output of the Formatter can now be used to trigger a similar Formatter in another equipment, connected via the "L" socket. This latter Formatter will respond with a serial ASCII message which is routed to the ASCII input pin of the GSDA/1 Formatter, and will appear at the ASCII output pin as an extension of the locally-generated message.

A logic 0 applied to the "Reset" input of the Formatter will always stop the output sequence and cause a jump back to the beginning of the program.

TECHNICAL DESCRIPTION

POWER SUPPLY ARRANGEMENTS

A type PS/5C Power Supply module is fitted. The 3-pin mains connector at the rear of this module is connected via the mains 3A fuseholder and an interference suppressor (fitted in a screened box immediately behind the connector) to pins 1 and 2 of the 24-way socket at the front. From pins 1 and 2 the mains passes to the ON/OFF switch on the front panel. From the switch, mains is fed back to pins 5 and 6 of the 24-way socket, and also to the two "Powercard" modules, which supply +15V and −15V respectively.

The GSDA/1 is normally arranged to work from 230V mains, but by changing connections as shown in the table on the System Diagram it can be made to work from 115V mains.

The PS/5C produces an unregulated d.c. voltage of about 10 or 11V, which is fed to three individually-fused output pins in the 24-way socket (pins 21, 22 and 23). The three outputs may be monitored at the fuseholders, which are easily accessible from the rear of the module. The unregulated d.c. is also connected via a current-limiting resistor to pin 17 of the socket whence it supplies the LED power indicator.

Two of the PS/5C outputs are used to supply two type PS/7A units, each of which contains an integrated voltage regulator capable of delivering up to 3A at 5V. The regulated outputs of these units form the V_{cc} supplies to the logic circuits.

The "Powercard" units supply +15V and −15V respectively with a rated output of 500mA each. In the event of a fault either unit can be removed by first unscrewing two M3 fixing screws accessible on the underside of the frame and then carefully withdrawing the unit to the rear, when it will disengage from its connecting socket. Access to the wiring side of the two sockets (should this be necessary) may be obtained by removing the safety cover, which is held in place by a single M3 screw.

COUNTER AND CONTROL BOARD

Area Gate pulses are amplified, inverted, and limited by the circuit of TR1, whose output is fed from the board for use elsewhere in the GSDA/1. Leading edges of the inverted area gate pulses trigger and re-trigger monostable IC 4b, whose output pulse width is set to a nominal value of 6 ms. IC 4b generates the "busy" pulse, which commences with the leading edge of the first area gate pulse and continues until about 6 ms. after the last pulse.

A stabilised potential of approximately +11V is produced across Zener Diodes D6 and D7, and this is reduced by resistors R4 and P1, to give precisely 10V across the Strike Count Threshold Potential potentiometer. The moving contact of the potentiometer is connected to the non-inverting input of amplifier IC2, which behaves as a level detector. During routine maintenance a digital voltmeter may be used to check both the 10V level (at TP6), and the voltage from the moving contact (at TP11).

The Video Signal is fed through voltage follower IC1 to the inverting input of IC2. Diodes D1, D2 and D3 conduct when the video signal is negative with respect to the threshold potential, thus ensuring that the output potential can never be more than about 1.5V more positive than the threshold potential, and hence preventing the amplifier going into saturation. Whenever the video signal exceeds the threshold potential, however, the diodes cut off and the output goes to about −0.6V, being limited by conduction of diode D4.

Should the video threshold be exceeded during an area gate pulse, a logic 1 will be generated by IC 3a, and this will set the latch formed by IC 3b and IC 3c. The latch will then remain set until cleared by the termination of the area gate pulse. Setting of the latch causes IC 4a to trigger, generating a 5μs "regenerated video" pulse.

IC9 and IC10 are two BCD counters which are always set to zero on the occurrence of the leading edge of the "busy" signal, which is differentiated by C11 and R20. Thereafter they count the "regenerated video" pulses and thus produce the strike count data in parallel BCD form.

The Camera Control Circuit operates as follows: IC8 is an oscillator whose frequency is adjusted by means of P2 to a value of approximately 2 Hz. Application of a logic 0 to the "reset" input of IC8 (pin 4) inhibits oscillation. The oscillator output pulses are counted by IC7, which is a BCD counter. The BCD output from IC7 is converted to a 1-of-10 signal by IC6, one of whose outputs (depending upon the BCD data) will always be logic 0, whilst the other nine outputs are switched to an open circuit state.

When the control switch is in the "off" position the oscillator will operate until IC7 reaches a count of 7, at which point a logic 0 will appear at pin 9 of IC6, forcing IC5b to output logic 1, and hence IC5a to output logic 0, which stops the oscillator. At this time also IC3d outputs logic 0 which lights the "Ready" indicator.

If the control switch is now momentarily operated to the "single shot" position, IC5c will output a logic 1, which will immediately set the counter to a count of 9. This will clear the logic 0 from pin 9 of IC6, and hence extinguish the "Ready" indicator and clear the set-to-nine pulse. The oscillator will still be disabled, however, because the "8" output from pin 11 of IC7 will now be at logic 1. The circuit will remain in this state until the next "busy" pulse occurs and resets IC7 to zero. The oscillator will then be enabled until IC7 once again reaches a count of 7.

If the control switch is in the "Repetitive" position the oscillator will not be stopped when a count of 7 is reached but will continue to a count of 8, when it will be stopped by the appearance of a logic 1 at pin 11 of IC7. The circuit will remain in this state until the next "busy" pulse resets IC7 and the sequence begins again.

The coils of the shutter and film advance relays are connected to the outputs of IC6 in such a way that the shutter relay is operated whenever the count is 0, 1, 8 or 9, whilst the film advance relay is operated when the count is 3, 4, 5 or 6.

VIDEO ISOLATION BOARD

The video signal is inverted and amplified approximately 10 dB by amplifier IC1. Potentiometer P1 is an offset nulling control, and should be adjusted to give 0 volts at TP10 when TP9 is grounded by shorting to TP1.

The circuit of IC3 and IC4 forms an inverting amplifier whose gain should be adjusted by means of P2 so that the overall gain from TP9 to TP11 is 20 dB when TP11 is loaded with 75Ω to ground.

The circuits of IC5 and 6, IC7 and 8, IC9 and 10, and IC11 and 12 are identical to that of IC3 and 4 (except for a minor difference in the case of IC11) and their gains should be adjusted to the same value.

A positive bias from the Pedestal Amplitude control is added to the input signal of IC5 except during the occurrence of area gate pulses, when the bias is pulled down to the logic 0 level through diode D2. This results in the output of IC6 being offset in a negative direction by an amount dependant upon the setting of the control, except during area gate pulses.

The circuit of TR1, TR2, TR3, TR4 and TR5 forms an analogue gate. Inverted area gate pulses switch TR1 off, which in turn switches TR2 and TR3 off. This causes TR4 to be switched on, allowing the inverted video signal from IC1 to be fed to IC2, whilst TR5 is switched off, presenting a high impedance to ground. When area gate pulses are not present, TR4 is turned off, whilst TR5 presents a low impedance to ground.

IC2 is a voltage follower whose output is the inverted "gated video" signal. This signal is used to drive the three output stages comprising IC7 and 8, IC9 and 10, and IC11 and 12.

The gated video signal to IC11 is mixed with the YCH signal at the junction of R46 and R47. (YCH is the vertical component of the character display signal). During the character display the YOS input falls to approximately 0V, thereby switching off TR6 and causing the character shift voltage across C4 to fall to some negative value dependant upon the setting of the Character Shift control potentiometer. This character shift voltage is passed to the non-inverting input of IC11 through D5. When the character display is not being generated the YOS input rises to about +1.75V, switching TR6 on and raising the character shift voltage almost to 0V. This voltage is insufficient to cause any appreciable conduction through D5, and the non-inverting input of IC11 is therefore effectively grounded through R49.

IC13 and IC14 constitute a non-inverting output amplifier for the X signal. The overall gain is approximately unity provided the output is loaded with 75Ω.

Similarly, IC15 and IC16 constitute a non-inverting output amplifier for the Beam Profile signal. The gain of this circuit should be adjusted to unity when loaded with 75Ω, by means of the gain control P7.

VIDEO MEASUREMENT BOARD

The circuit of IC1, TR1 and IC2 forms a peak detector. During area gate pulses D1 cannot conduct and therefore the emitter voltage of TR1 will follow any positive-going transition in the video signal. The potential across C3 will therefore rise to whatever peak value the video signal reaches, but cannot then fall when the video signal starts to go down again because D4 will not conduct in the reverse direction. IC2 is a voltage follower with a very high input resistance. Its output follows the voltage across C3, and feeds this voltage back to the inverting input of IC1, causing the circuit to have an overall gain of unity. The tendency of IC1 to produce overshoot is reduced by additional feedback through R4, C2 and D2 (the voltage drop across D2 during conduction approximately equalling, and therefore cancelling, the drop across D4). As a further precaution against overshoot, the inclusion of R7 in

series with C3 both slows down the charging time of C3 and increases the slew rate of the signal to IC2. D3 introduces negative feedback when the input signal falls below its previous peak value and hence prevents IC1 going into saturation.

The inverted area gate pulses are applied to pin 13 of IC5, causing the level at TP10 to go to logic 1 as soon as a pulse occurs. This switches TR4 on, pulling its collector up to just above ground potential, and thereby switching TR5 off. C3 can now be charged through D4, as described above. On the termination of an inverted area gate pulse the monostable IC6a is triggered, and produces a pulse of about 25μs duration which switches off TR6, and hence TR7, thereby removing the negative bias from the gate of TR2 and allowing it to conduct. C4 now charges or discharges until the potential across it is equal to the voltage stored on C3. (Note that during all this time TR3 is switched off due to the occurrence of a "busy" pulse).

When the 25μs pulse from IC6a terminates, TR2 switches off again, whilst the peak voltage remains stored on C4 until after the occurrence of the next area gate pulse. The termination of the 25μs pulse also triggers IC6b, causing a 0-to-1 transition at TP9 6μs later. This clocks IC5a and IC5b causing TP10 and TP2 to fall to logic 0. TR4 now switches off, allowing C3 to discharge through TR5 at a constant rate determined by the setting of P1. Simultaneously, because the counter IC7 is no longer held in a reset state, it starts to output a square wave having a frequency of one-sixteenth of the crystal oscillator frequency.

When C3 has discharged, amplifier IC4 (which behaves as a level detector) outputs a logic 0 voltage which resets IC5b, hence holding IC7 once again in the reset state. The number of cycles of the square wave output by IC7 is proportional to the time taken to discharge C3, which in turn is proportional to the voltage originally stored on C3.

IC9, 10, 11 and 12 constitute a digital peak detector circuit, which counts the number of pulses in each burst from IC7, and ultimately outputs a BCD number corresponding to the longest burst observed. The circuit works as follows:

IC11 and IC12 are both reset to zero on the occurrence of the leading edge of the "busy" pulse (which is differentiated by C7 and R27 and R28). The inverted area gate pulses are fed directly to the Load inputs of IC9 and 10, and therefore these counters will be set to whatever number is output by IC11 and 12 (i.e. zero during the first area gate pulse). IC9 and 10 are arranged to count downwards except when they are in the zero state, in which state the count pulses propagate through and appear at the Borrow output of IC10, whence they are fed back in inverted form to the Clear inputs, preventing any further counting. The Borrow pulses are, however, counted by IC11 and IC12, and thus after the first burst of pulses IC11 and 12 will store the value of that burst. This value is then transferred to IC9 and 10 by the next area gate pulse, and therefore Borrow pulses will now only be generated if the burst length exceeds the previous value.

The total number of pulses output by IC7 is counted by IC13, 14, 15 and 16, whose output thus represents the sum of the amplitudes of all video pulses observed.

TIME DECODER

The Time coded signal is converted to TTL levels by a transistor inverter. Every transition of the signal results in a positive-going pulse at IC2 pin 11, which triggers a pulse at IC4 pin 4. The back edge of this pulse results in another pulse at IC4 pin 5, enabling IC2 pin 9. Any signal transition occurring during this second pulse will result in IC5 pin 9 being set high, and at the back edge of the pulse this high state will be shifted into the first stage of shift register IC8, IC5 pin 9 being simultaneously cleared. The outputs of IC8 are continuously examined by IC7 for the synchronising code. Also the output from the final stage of IC8 passes into the remaining stages of the shift register, ICs 9, 10 and 11.

When the synchronising code is detected, IC7 pin 8 goes low, assuming that the Flag signal is low, and IC3 pin 10 then goes high when IC3 pin 9 goes low, clocking IC5 pin 5 high and pin 6 low. When the synchronising code is detected a second time, IC5 pin 5 goes low and pin 6 high, triggering IC6 and clocking the contents of shift register ICs 9, 10 and 11 into the latches ICs 12, 13, 14 and 15. Whilst IC6 is firing it prevents IC5 pins 5 and 6 from responding to further clock pulses (i.e. to the final synchronising pattern).

If the Flag signal is high, IC3 pin 4 will be held low and IC7 will not respond to further synchronising codes until the Flag signal goes low again.

CHARACTER GENERATOR

An instruction sequence for the generation of each different character is stored in the form of sixteen consecutive 4-bit words in the read-only memory (ROM) IC5, which has a total capacity of 256 4-bit words. To generate any one of the sixteen possible characters, the four most significant bits of the ROM address (E, F, G and H) are held constant at a value unique to that character whilst the four least significant bits (A, B, C and D) are incremented at a constant rate. Each instruction word is a command to the beam in the oscilloscope tube to travel in a certain direction and to switch either on or off whilst doing so. Eight different directions are possible, i.e. North, South, East, West, North-East, North-West, South-East and South-West. The direction is defined by the three bits, Y_1, Y_2 and Y_3, whilst the fourth bit, Y_4, defines the beam off/on status. The direction data is converted by IC10, IC11 and IC13 into digital signals that control the analogue voltage generating circuits, which in their turn produce the appropriate X and Y output waveforms.

The X analogue circuit (TR1-5) is virtually identical to the Y circuit (TR6-10), and therefore only the operation of the X circuit will be described here.

The bases of TR4 and TR5 are each connected to stabilised voltage sources (i.e. zener diodes D2 and D4). Thus when TR3 is switched off TR4 will deliver a steady positive constant current to C5a and C5b, and when TR2 is switched off TR5 will deliver an equal but negative current to C5a and C5b. Thus the potential across C5 may be made to increase at a steady rate by switching off TR3, or to decrease at the same steady rate by switching off TR2, or to remain constant at whatever its value happens to be by not switching off either TR2 or TR3.

The value of the current delivered by TR4 should be adjusted by means of P1 to equal that delivered by TR5. When character generation is not in progress TR3 is switched off, (i.e. TR4 is on), but now TR11 is switched on, drawing current through D1 and hence setting the potential across C5 to a starting value determined by the setting of P2.

Since the XCH and YCH outputs are both in inverted form, voltage changes in the positive direction on C5 or on C6 will ultimately cause the beam to be deflected leftwards or downwards. The following table relates the beam deflection to the control data.

Beam Deflection	Voltage change		Status				Data		
	C5	C6	TR1	TR3	TR6	TR8	Y_1	Y_2	Y_3
↑	0	↓	ON	ON	OFF	ON	1	1	0
↙	↓	↓	OFF	ON	OFF	ON	1	1	1
→	↓	0	OFF	ON	ON	ON	1	0	0
↘	↓	↑	OFF	ON	ON	OFF	1	0	1
↓	0	↑	ON	ON	ON	OFF	0	0	0
↙	↑	↑	ON	OFF	ON	OFF	0	0	1
←	↑	0	ON	OFF	ON	ON	0	1	0
↖	↑	↓	ON	OFF	OFF	ON	0	1	1

Instruction bit Y_4 is logic 0 for "beam on", and logic 1 for "beam off". The sequence of instructions controlling the generation of any character assume a starting position for the beam which is always in the same place relative to the character position, and lead the beam eventually to a finishing position which will be in the same place relative to the next character position. The full ROM program is listed in Appendix I.

The operation of the rest of the circuit of the Character Generator is described as follows:

Inverters IC 7c, d, and e together form an oscillator whose frequency is dependent upon the value of C4, and is nominally 330 kHz. Oscillation can be stopped by the application of a logic 1 to the input of IC 7f. When the circuit is at rest the counter IC8 is at a count of 8, causing IC 12d to output logic 0, and hence IC 12c to output logic 1, thereby inhibiting the oscillator and resetting IC6 to zero.

When the trailing edge of the "busy" pulse occurs this triggers monostable IC9, causing the Status (B) output

to rise to logic 1 (which prevents further updating of the time data) and the character offset outputs to fall to 0V (which positions the beam ready for character display). After about 20μs the pulse from IC9 terminates, and the back edge of the pulse (differentiated by C2 and R4) resets IC8 to zero. IC 12d now outputs a logic 1, and since the termination of the pulse from IC9 is delayed by R5 and C3 the Status (B) and Character Offset outputs remain in the logic 1 and 0 states respectively, unaffected by transient conditions.

Data selectors IC1-4 select the data for the first digit and apply it to the ROM as the four most significant address bits. The oscillator is enabled and therefore the four least significant address bits of the ROM are now cycled from zero to 15, causing the ROM to output the appropriate sequence of sixteen instruction words. On completion of the sequence IC6 increments from a count of 15 to a count of zero, thereby incrementing IC8. The data selectors now select the data for the second digit, and the sequence continues as before. This cycle of events continues until IC8 reaches a count of 8 and brings the circuit to rest once again.

Note that the third and sixth data inputs (i.e. N = 2 and N = 5) are hard-wired at the rear of the edge connector to cause the generation of hyphen symbols.

INTERRUPTED RAMP GENERATOR

Inverters IC 2a, b, and c form an oscillator which constantly outputs pulses to IC 1c. During each area gate pulse, therefore, IC 1c outputs a burst of pulses which are counted by IC7, 8, 9 and 10. The counters are reset to zero except during the "busy" pulse, and therefore immediately prior to the trailing edge of each "busy" pulse the number accumulated in the counters will be proportional to the number of area gate pulses that have occurred and the length of the individual pulses, i.e. to the total time during which area gate pulses were active. The eight most significant bits of the count are latched into IC5 and 6 by the trailing edge of the "busy" pulse just before the counters are reset.

The circuit IC3, TR3 and IC4 generates a current which is inversely proportional to the magnitude of the data stored in IC5 and 6. The reason for this is as follows:

IC4 behaves as a current attenuator whose output current (flowing into pin 4) is proportional in magnitude to its input current (flowing into pin 14) times the value of the data input. Amplifier IC3 and TR3 form a negative feedback loop which always adjusts the input current so as to give a constant output current of approximately 16μA. Since input current x data is held constant, input current must therefore be inversely proportional to data.

Since the base current drawn by TR3 is neglible, the collector of TR3 forms a current sink (or negative current source) inversely proportional in value to the total active time of the area gate pulses. During area gate pulses the negative current from TR3 flows entirely into C5, but in the absence of area gate pulses it is diverted through TR2. The voltage waveform across C5 is therefore in the form of a negative-going interrupted ramp.

In the absence of a "busy" pulse TR5 is switched on, pulling the potential on C5 up to approximately +6V.

When the front panel control switch is thrown to the "Fix Ramp Rate" position this applies a logic 0 to IC 1d, thereby inhibiting further updating of the data stored by IC5 and IC6.

When the control switch is set to "Magnify" this sets IC5 and 6 to zero, causing TR3 to deliver a fixed constant current. (Positive excursion of the output of IC3 under this condition is limited by diode D1). Also, TR7 is now switched on, causing TR6 to deliver an additional constant current to C5. In this mode of operation TR5 is switched on all the time, except during area gate pulses. The waveform produced across C5 is therefore in the form of a negative-going sawtooth, returning to approximately +6V after each area gate pulse.

FORMATTER

Introduction

The control program is contained in a read-only memory, IC5, in the form of 32 8-bit characters. The instruction to be performed is selected by IC10 and decoded by ICs 11, 13 and 7. Data inputs are selected by ICs 1, 2, 3 and 4, and IC6 selects either Data or stored characters, all under program control. ICs 8 and 9 control the conversion from BCD to serial ASC11 code, and IC20 is the timing source.

Basic Operation

Assuming that operation begins with the Reset signal going low. This results in IC15 pin 5 being set low and the program counter, IC10, being cleared, IC5 being inhibited during all this.

Also, if the optional link to stop on external Reset is fitted, IC16 pin 9 will be set low, i.e. the Flag signal,

resulting in oscillator pulses from IC20 pin 6 being prevented from appearing at IC18 pin 3.

This state of affairs will persist until the Begin signal goes low, resulting in IC16 pin 9 and the Flag signal being set high and oscillator pulses now being routed to IC17 pin 1 and IC19 pins 5 and 10.

This causes IC15 pin 5 to go high, selecting program step 1 in IC5, assuming that the repeat signal is high.

If the repeat signal is low, IC15 pin 5 will remain low, selecting program step 0. A short pulse is triggered at IC17 pin 13, followed by a second pulse at IC17 pin s 5 and 12. Further operation depends on the stored program as follows:—

Send Character

Code is IC5 pin 9 low, IC5 pins 1, 2, 3, 4, 5, 6 and 7 dependent on character to be transmitted.

IC5 pin 9 being low forces IC6 to select inputs on pins 2, 5, 14 and 11 and causes a high to appear on IC13 pins 3 and 6, taking IC11 pin 12 high and thus disenabling IC11. IC7 pin 12 is taken low and IC9 pin 7 high. When the pulse from IC17 pin 5 appears at IC9 pin 6, IC9 is set to binary 9, i.e. pins 12 and 11 go high and pins 9 and 8 go low, resulting in IC14 pin 3 going low. This causes oscillator pulses to be routed to IC9 pin 6 and IC18 pin 6. IC9 pin 11 stays high for one oscillator cycle keeping IC8 pin 5 and IC14 pin 8 low, and hence generating the "start" bit required by the serial code format. On the next oscillator pulse the counter IC9 resets to all zeros, selecting IC8 pin 4 which in turn depends on the state of IC5 pin 1, i.e. bit 1 of the code to be transmitted. On subsequent oscillator pulses, IC9 and IC8 select bits 2-7 of the code. The serialised data, as well as going to IC14 pin 8 and out, are used to control the count inputs, pins 1 and 4, of IC15. At the end of the serial data the state of IC15 pin 3 depends on whether the number of "ones" in the code was odd or even, and either this state or its inverse can be selected by means of a wire link and fed to IC8 pin 12, where it is selected and transmitted after bit 7 as a parity bit.

At a count of 8, IC14 pin 3 goes high again, cutting off the supply of clock pulses to IC9 and raising IC17 pin 2.

Marker Y

Code is IC5 pin 9 high, pins 5, 6 and 7 low. As a result of the above code, IC11 selects pin 1 and then, when the pulse is generated at IC17 pin 5 it is routed to IC11 pin 1 and becomes the Marker Y pulse. The program counter then increments as normal.

Marker Z

Code is IC5 pins 6 and 9 high, 5 and 7 low. This is generated exactly as was Marker Y and appears at IC11 pin 3.

Send Data

Code is IC5 pins 7 and 9 high, 5 and 6 low. IC6 is made to select as inputs pins 3, 6, 13 and 10, as pin 1 is high, and ICs 1, 2, 3 and 4 select an input for routing to IC6 dependent upon the state of IC5 pins 1, 2, 3 and 4.

If, however, the Blank signal is low, the enable inputs, pins 9, of ICs 1, 2, 3 and 4 go high resulting in their outputs being high regardless of the state of their data inputs. This results in a space character being transmitted, since IC8 pin 15 is also held low via IC7 pins 10 and 13 and IC14 pin 6. Assuming the Blank signal high, the selected data inputs routed via IC6 to IC8 pins 4, 3, 2 and 1, but IC8 pins 15 and 14 are held high because of the low state of IC5 pins 5 and 6. IC9 is set to 9 (i.e. started) by a pulse from IC11 pin 2 derived in the usual way from IC17 pin 5 (i.e. see Marker Y).

Send Space and Set Zero Suppression

Code is IC5 pins 5, 7 and 9 high, 1, 2, 3, 4 and 6 low. The pulse from IC17 pin 5 is routed via IC11 pin 6 and sets IC16 pin 6 low, resulting in IC8 pin 15 going low. Also, since IC5 pin 6 is low, IC8 pin 14 is high. IC5 pins 1, 2, 3 and 4 are low causing ICs 1, 2, 3 and 4 to select pin 8, i.e. OV, and resulting in IC8 pins 4, 3, 2 and 1 being low. Therefore a space code exists on the inputs of IC8 and will be transmitted in the normal way. IC16 pin 6 remains low during subsequent Send Data cyles, transmitting space codes instead of zero due to the fact that IC8 pin 15 is forced low by the low on IC16 pin 6, until non-zero Data appears, resulting in one or more of IC7 pins 3, 2, 5 and 6 going high, clocking IC16 pin 6 high. Operation is then back to normal.

Clear Zero Suppression

Code is IC5 pins 5, 6 and 9 high, pin 7 low. The pulse from IC17 pin 5 is routed via IC11 pin 7 to reset IC16 pin 6 high.

End

Code is IC5 pins 5 and 9 high, 6 and 7 low. The pulse from IC17 pin 5 is routed via IC11 pin 5 and holds IC16 pin 12 low during a clock transition at IC16 pin 11. This results in IC16 pin 9, and hence the Flag signal, going low and preventing oscillator pulses from reaching IC17.

Jump To Program Step O

Code is IC5 pins 5, 6, 7 and 9 high. The pulse from IC17 pin 5 is routed via IC11 pin 9 to clear the program counter to zero. Instruction step zero will, however, only be performed next if the repeat signal is being held low and thus preventing IC15 pin 5 from changing state.

Conditional Jump

Code is IC5 pins 6, 7 and 9 high, pin 5 low. The pulse from IC17 pin 5 is routed via IC11 pin 4 and at its back edge, provided that the Jump Enable signal is high, the program counter is loaded with the binary number present at IC5 pins 1, 2, 3 and 4. If the Jump Enable signal is low, the loading pulse will not appear at IC13 pin 11 and the jump instruction will be totally ignored.

Interrupt Control Input

If the Interrupt signal goes low at any time, the Formatter will finish executing the current instruction and will then stop, since IC17 pin 13 is clamped high. As soon as the Interrupt signal goes high a pulse will be triggered at IC17 pin 13 and operation will resume as normal.

For a listing of the ROM program used in the GSDA/1 see Appendix II.

APPENDIX I

ROM PROGRAM FOR CHARACTER GENERATOR

Word No.	Y_1	Y_2	Y_3	Y_4	Character
0	1	1	0	0	
1	1	1	0	0	
2	1	1	1	0	
3	1	0	0	0	
4	1	0	1	0	
5	0	0	0	0	
6	0	0	0	0	
7	0	0	0	0	
8	0	0	1	0	0
9	0	1	0	0	
10	0	1	1	0	
11	1	1	0	0	
12	1	0	0	1	
13	1	0	0	1	
14	1	0	0	1	
15	1	0	0	1	
16	1	1	0	1	
17	1	1	1	1	
18	1	1	1	0	
19	0	0	0	0	
20	0	0	0	0	
21	0	0	0	0	
22	0	0	0	0	
23	0	0	0	0	
24	0	1	0	1	1
25	1	0	0	0	
26	1	0	0	0	
27	0	1	0	1	
28	1	1	0	1	
29	1	1	0	1	
30	1	0	0	1	
31	1	0	0	1	
32	1	1	0	1	
33	1	1	0	1	
34	1	1	1	0	
35	1	0	0	0	
36	1	0	1	0	
37	0	0	0	0	
38	0	0	1	0	
39	0	0	1	0	
40	0	0	1	0	2
41	1	0	0	0	
42	1	0	0	0	
43	1	0	0	0	
44	0	1	0	1	
45	1	1	0	1	
46	1	1	1	1	
47	1	0	0	1	

Word No.	Y_1	Y_2	Y_3	Y_4	Character
48	0	0	0	1	
49	1	0	1	0	
50	1	0	0	0	
51	1	1	1	0	
52	1	1	0	0	
53	0	1	1	0	
54	0	1	0	1	
55	0	1	1	1	
56	1	1	1	0	3
57	1	0	0	0	
58	1	0	1	0	
59	0	0	1	0	
60	0	1	0	0	
61	1	0	0	1	
62	1	0	0	1	
63	1	0	1	1	
64	1	0	0	1	
65	1	0	0	1	
66	0	0	0	0	
67	0	0	0	0	
68	1	1	0	1	
69	1	0	0	1	
70	0	1	0	0	
71	0	1	0	0	
72	0	1	0	0	4
73	1	1	0	0	
74	1	1	1	0	
75	1	1	1	0	
76	1	1	1	0	
77	0	0	1	1	
78	1	0	1	1	
79	1	0	1	1	
80	0	0	0	1	
81	1	0	1	0	
82	1	0	0	0	
83	1	1	1	0	
84	1	1	0	0	
85	0	1	1	0	
86	0	1	0	0	
87	0	1	0	0	
88	1	1	0	0	5
89	1	1	0	0	
90	1	0	0	0	
91	1	0	0	0	
92	1	0	0	0	
93	0	0	0	1	
94	1	0	1	1	
95	0	0	0	1	

Word No.	Y_1	Y_2	Y_3	Y_4	Character
96	1	1	1	0	
97	1	0	0	0	
98	1	0	1	0	
99	0	0	0	0	
100	0	0	1	0	
101	0	1	0	0	
102	0	1	1	0	
103	1	1	0	0	
104	1	1	0	0	6
105	1	1	0	0	
106	1	1	1	0	
107	1	0	0	0	
108	1	0	1	0	
109	1	0	0	1	
110	0	0	0	1	
111	0	0	0	1	
112	1	1	0	1	
113	1	1	0	1	
114	1	1	0	1	
115	1	0	0	0	
116	1	0	0	0	
117	1	0	0	0	
118	0	0	0	0	
119	0	0	1	0	
120	0	0	1	0	7
121	0	0	0	0	
122	0	0	0	0	
123	1	1	0	1	
124	1	1	0	1	
125	1	0	0	1	
126	1	0	0	1	
127	1	0	0	1	
128	1	1	1	1	
129	0	0	1	0	
130	0	0	0	0	
131	1	0	1	0	
132	1	0	0	0	
133	1	1	1	0	
134	1	1	0	0	
135	0	1	1	0	
136	0	1	0	0	8
137	0	1	1	0	
138	1	1	1	0	
139	1	0	0	0	
140	1	0	1	0	
141	0	0	1	0	
142	1	0	1	1	
143	1	0	0	1	

Appendix 1 (cont.)

Word No.	Y_1	Y_2	Y_3	Y_4	Character
144	0	0	0	1	
145	1	0	1	0	
146	1	0	0	0	
147	1	1	1	0	
148	1	1	0	0	
149	1	1	0	0	
150	1	1	0	0	
151	0	1	1	0	
152	0	1	0	0	9
153	0	0	1	0	
154	0	0	0	0	
155	1	0	1	0	
156	1	0	0	0	
157	1	1	1	0	
158	0	0	0	1	
159	1	0	0	1	
160	1	0	0	1	
161	1	0	0	1	
162	1	0	0	1	
163	0	1	0	1	
164	0	1	0	1	
165	0	1	0	1	
166	1	0	0	0	
167	1	0	0	0	
168	1	0	0	0	Hyphen
169	0	1	0	1	
170	0	1	0	1	
171	0	1	0	1	
172	1	0	0	1	
173	1	0	0	1	
174	1	0	0	1	
175	1	0	0	1	
176	1	0	0	1	
177	1	0	0	0	
178	0	0	0	0	
179	0	1	0	0	
180	1	1	0	0	
181	1	0	1	0	
182	0	1	0	1	
183	1	1	1	0	
184	0	0	0	1	Decimal Point
185	0	0	0	1	
186	1	0	0	1	
187	1	1	0	1	
188	1	1	0	1	
189	1	1	0	1	
190	1	0	0	1	
191	0	0	0	1	

Word No.	Y_1	Y_2	Y_3	Y_4	Character
192	0	0	0	1	
193	0	0	0	1	
194	0	0	0	1	
195	1	0	0	1	
196	1	1	1	0	
197	1	1	0	0	
198	0	1	0	0	
199	0	0	0	0	
200	1	0	0	0	Comma
201	0	1	1	0	
202	0	0	0	1	
203	1	1	1	0	
204	0	1	0	1	
205	1	0	0	1	
206	1	0	0	1	
207	1	1	1	1	
208	1	1	0	1	
209	1	1	0	1	
210	1	1	1	1	
211	1	1	1	1	
212	0	0	1	0	
213	0	0	0	0	
214	0	0	0	0	
215	0	0	0	0	
216	0	0	0	0	Open Bracket
217	0	0	0	0	
218	1	0	1	0	
219	0	1	1	1	
220	1	1	0	1	
221	1	1	1	1	
222	1	0	0	1	
223	1	0	0	1	
224	1	1	1	1	
225	1	1	1	1	
226	1	1	0	1	
227	0	1	1	1	
228	1	0	1	0	
229	0	0	0	0	
230	0	0	0	0	
231	0	0	0	0	
232	0	0	0	0	Close Bracket
233	0	0	0	0	
234	0	0	1	0	
235	1	1	1	1	
236	1	1	0	1	
237	1	1	0	1	
238	1	0	0	1	
239	1	0	0	1	

Word No.	Y_1	Y_2	Y_3	Y_4	Character
240	1	0	0	1	
241	1	0	0	1	
242	1	0	0	1	
243	0	1	0	1	
244	0	1	0	1	
245	0	1	0	1	
246	1	0	0	1	
247	1	0	0	1	
248	1	0	0	1	Space
249	0	1	0	1	
250	0	1	0	1	
251	0	1	0	1	
252	1	0	0	1	
253	1	0	0	1	
254	1	0	0	1	
255	1	0	0	1	

APPENDIX II

ROM PROGRAM FOR FORMATTER

Instruction No.	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	Hexadecimal Notation
0	1	0	0	0	0	0	0	0	8 – 0
1	0	1	0	1	1	1	1	1	5 – 15
2	0	1	0	1	1	1	1	1	5 – 15
3	1	1	0	1	0	0	0	0	13 – 0
4	1	1	0	0	0	0	0	1	12 – 1
5	1	0	1	1	0	0	0	0	11 – 0
6	1	1	0	0	0	0	1	0	12 – 2
7	1	1	0	1	0	0	0	0	13 – 0
8	1	1	0	0	0	0	1	1	12 – 3
9	1	0	1	1	0	0	0	0	11 – 0
10	1	1	0	0	0	1	0	0	12 – 4
11	1	1	0	1	0	0	0	0	13 – 0
12	1	1	0	0	0	1	0	1	12 – 5
13	1	1	0	0	0	1	1	0	12 – 6
14	1	1	0	0	0	1	1	1	12 – 7
15	1	0	1	1	0	0	0	0	11 – 0
16	1	1	0	0	1	0	0	0	12 – 8
17	1	0	0	1	0	0	0	0	9 – 0
18	1	1	1	1	0	0	0	0	15 – 0
19 ↓ 31	ALL ZEROS								0 – 0

FRONT PANEL ASSEMBLY

Part No.	Qty.	Description
		Specially Machined Items
	1	Front Panel
	1	Front Sub-Panel
	1	Cable Clamping Bracket
		Other Components – See D202023 for assy. details
		(A) Sub-Panel Assembly
004620	2	Screw, M3 x 8, panhead
004991	2	Washer, S/p, M3
003185	1	Solder tag, 6BA
004893	2	Nut M3
007756	2	Switch, paddle, 3-position
008176	1	Switch, paddle, 3-position, biased
007742	1	Switch, paddle, 2-position
	8	Spring washer, (included in paddle switch kits)
004592	8	Screw, M2 x 8, panhead
008022	8	Spacer, $^1/_8$" x 8BA cl.
008540	2	Min Maka Switch
008904	2	Switch, wafer, 4-pole, 3-way
008561	1	Switch, wafer, 3-pole, 4-way
	4	Spacer, M2. (From Min Maka Switch)
004984	4	Washer, S/p, M2
004886	4	Nut M4
004641	2	Screw, M3 x 16, p/h
		(B) Front Panel Assy
000441		Switch, DPST, with Hex. nut, Knurled nut, & keying washer
000413	2	LED, Red
008582	1	LED, Yellow
008596	1	LED, Green
		(C) Fixing Sub-Panel to Front Panel
008631	1	Potentiometer 470Ω
008603	3	Potentiometer 4K7
008363	1	Potentiometer 10K
008526	1	Precision potentiometer. 1K0
008533	1	10-turn dial mechanism
003143	1	Knob with skirt, 28.4mm
003150	1	Knob with skirt, 41.9mm
006083	5	Knob, 14.5mm
006104	5	Knob cap
008204	5	Knob skirt, lined

REAR CONNECTOR BRACKET ASSEMBLY

Part No.	Qty.	Description
		Specially Machined Items
	1	Connector Mounting Bracket
	2	Board Retainer
007196	1	Screw Lock Block
007161	2	Hinge Fixing Block
007154	2	Hinge
		Other Components
008050	2	Plug, Fixed, 5-way, X-L Type
006286	1	Socket, Fixed, 5-way, X-L Type
008071	14	Socket, BNC, Flange Mounting Type
004690	1	Screw, M4 x 30, panhead
004774	67	Screw, M3 x 8, CSK Head
004781	6	Screw, M3 x 12, CSK Head
004620	4	Screw, M3 x 8, Pan head
004893	66	Nut, M3
004991	66	Washer, S/P, M3
003185	15	Solder Tag, 6BA
	22cm	Self-adhesive foam strip

FRAME ASSEMBLY

Part No.	Qty.	Description
		Specially Machined Items
007511	1	Frame, Modified
	1	PS/5C
	2	Connector Mounting Bracket
007175	1	Hinge Mounting Bracket
007182	1	Screw Lock Block
	1	Cable Clamping Rail
	1	Rear Connector Bracket Assy
	1	Power Card Base Plate
	1	Power Card Conn. Mtg. Panel
	2	Power Card Socket
004676	4	Screw, M4 x 12, CSK Head
		Other Components – See D202023 for assembly details
000035	36	Chassis Guide
		Edge Connector Assemblies
005523	5	Edge Connector, single sided
005901	2	Edge Connector, double sided
004473	7	Index key
004466	14	Clip
000245	14	Screw, 6BA x ½" Pan head
000315	14	Washer, plain, 6BA
		PS/7A Socket Assemblies
007455	2	Socket, 8-way, in-line
004606	4	Screw, M2 x 12, Pan head
004935	4	Washer, Plain, M2
004984	4	Washer, S/p, M2
004886	4	Nut, M2
000252	4	Screw, 6BA x $^{5}/_{16}$", pan head
		Hinge Mounting Bracket Assy
004634	4	Screw, M3 x 12, pan head
004102	4	Spacer , $^{1}/_{8}$" x 6BA C1
004991	4	Washer, S/p, M3
004893	4	Nut, M3
		Screw Lock Block Assembly
004613	1	Screw, M3 x 6, Pan head
004991	1	Washer, S/p, M3
		Power Card Base Plate Assy
004116	4	Spacer, ¼" x 6BA cl.
004991	4	Washer, M3, S/p
004893	4	Nut, M3
		Power Card Connector Panel Assembly
007196	1	Insert, Threaded M3
004655	4	Screw, M3 x 25, Pan head (reduce to 20mm)
004130	4	Spacer, ½" x 6BA cl.
004991	4	Washer, S/p, M3
004893	4	Nut, M3
000252	4	Screw, 6BA x $^{5}/_{16}$", pan head
003185	1	Solder tag, 6BA
004991	1	Washer, S/p, M3
		Cable Clamping Rail Fixing
000210	4	Screw, 6-32UNC x ½", Taptite, pan head

Part No.	Qty.	Description
		Rear Connector Bracket Fixing
004662	2	Screw, M4 x 8, pan head
004900	2	Nut, M4
		Miscellaneous
003185	1	Solder Tag, 6BA
000252	1	Screw, 6BA x $^{5}/_{16}$" pan head
004991	1	Washer, S/p, M3
004662	4	Screw, M4 x 8, pan head

COUNTER & CONTROL BOARD

Part No.	Qty.	Description
		Miscellaneous
008260	1	PCB ready for assy
006664	2	Bus Bar
007714	1	Handle with test points
003045	24	Pin, solder
007525	1	Transistor mounting Pad, T018
008295	2	IC Mounting Pad, 8-pin DIL.
006440	2	Relay, Type 24
006454	2	Socket
006475	2	Clip
008624	2	Potentiometer, Type 43P 100Ω, cermet, multiturn
		Integrated Circuit
003521	2	SN7402N
005341	1	SN7445N
003626	3	SN7490AN
006986	1	SN74123N
008183	1	LM310H
008190	1	LM318H
008351	1	NE555V
		Capacitors
002394	1	18pF, 160V, Polystyrene
002541	1	330pF, 160V, Polystyrene
002604	2	1000pF, 160V, Polystyrene
002205	1	0.047μF, 250V, Polyester
002261	4	0.47μF 100V, Polyester
002275	1	0.68μF, 100V, Polyester
002282	1	1.0μF, 100V, Polyester
		Transistors & Diodes
002870	1	BSX20
002912	8	1N914
005712	2	BZY88 – C5V6
002926	1	0A47
		Resistors (½W, 5%, Carbon Film)
000623	1	18Ω
000763	1	68Ω
000805	2	100Ω
000840	1	150Ω
000896	2	240Ω
000966	1	470Ω
001043	1	1K
001113	1	2K
001141	2	2K7
001225	4	5K6
001281	1	10K
001344	1	18K
001400	1	33K
001806	1	1M5
000840	2	150Ω

VIDEO ISOLATION BOARD

Part No.	Qty.	Description
		Miscellaneous
008253	1	PCB ready for assy
006664	3	Bus Bar
003045	10	Pins, solder
007525	6	Transistor Mounting Pads, T018
008295	16	IC Mounting Pad, 8-pin DIL
007714	1	Handle with test points
008363	6	10K Cermet Potentiometer
008372	1	100K Cermet Potentiometer
		Integrated Circuit
008211	7	LH0002CH
008190	8	LM318H
008225	1	ML741CT
		Capacitors
002261	2	0.47μF, 100V, Polyester
002464	1	68pF, 160V, Polystyrene
006293	1	0.047μF, 25V, Ceramic
006293	20	0.047μF, 25V, Ceramic
002093	1	100μF, 10V. Electrolytic
001995	2	470μF, 25V, Electrolytic
		Transistors & Diodes
002842	3	BCY70
006951	2	BFW10
002870	1	BSX20
002912	3	1N914
002926	1	0A47
005705	1	BZY 88 – C5V1
		Resistors (½W 5% carbon film)
00770	21	75Ω
008400	1	82Ω, 2%, metal oxide
000805	1	100Ω
001001	1	680Ω
001015	1	750Ω
008463	1	910Ω, 2%, Metal Oxide
001085	5	1K5
001106	7	1K8
001120	1	2K2
001141	1	2K7
001176	1	3K6
001204	1	4K7
001211	9	5K1
001260	1	8K2
001281	2	10K
001323	2	15K
001442	3	47K
001596	1	200K
001043	1	1K0
002401	1	22pF Capacitor, 160V, Polystyrene
002443	1	47pF Capacitor, 160V, Polystyrene
002534	1	270pF Capacitor, 160V, Polystyrene
001183	1	3K9Ω Resistor
002380	1	15pF Capacitor, 160V, Polystyrene

VIDEO MEASUREMENT BOARD

Part No.	Qty.	Description
		Miscellaneous
008274	1	PCB Ready for assy
006664	2	Bus Bar
007714	1	Handle with test points
003045	59	Pin, solder
007525	8	Transistor Mountain Pad, T018
008295	4	IC Mounting Pad, 8-pin, DIL
008155	1	Crystal Oscillator, 11.030MHz
003360	1	Potentiometer, Cermet, 5K multiturn
		Integrated Circuits
003535	1	SN7404N
003591	1	SN7474N
003626	6	SN7490AN
003633	1	SN7493AN
006986	1	SN74123N
005831	2	SN74192N
008183	2	LM310H
008190	2	LM318H
		Capacitors
002401	1	22pF, 160V, Polystyrene
002443	2	47pF, 160V, Polystyrene
002562	2	470pF, 160V, Polystyrene
002604	3	1000pF, 160V, Polystyrene
002646	1	2200pF, 160V, Polystyrene
002261	3	0.47μF, 100V, Polyester
002366	1	10pF, 160V, Polystyrene
006293	1	0.047μF, 25V, Ceramic
		Transistor & Diodes
002793	1	BC108
002842	3	BCY70
006951	2	BFW10
002870	2	BSX20
002912	7	1N914
005656	1	BZY88 – C3V3
005712	2	BZY88 – C5V6
		Resistors (5%, ½W, Carbon Film)
000581	1	12Ω
000672	1	30Ω
000770	1	75Ω
001043	4	1K
001085	3	1K5
001106	1	1K8
001113	1	2K
001120	1	2K2
001134	1	2K4
001141	3	2K7
001225	3	5K6
001281	3	10K
001421	2	39K
001561	1	150K
001596	1	200K
001603	1	220K
001323	1	15K
001680	1	470K

TIME DECODER

Part No.	Qty.	Description
		Miscellaneous
007630	1	P.C. Board ready for assembly
006664	3	Bus Bar
007714	1	Handle with Test Points
007525	2	Transistor Mounting Pad
003045	70	Pin, Solder
		Integrated Circuits
003514	1	SN7400N
003521	1	SN7402N
003563	1	SN7430N
003591	1	SN7474N
003640	1	SN74121N
006986	1	SN74123N
007084	1	SN74132N
005334	4	SN74164N
007812	4	SN74174N
		Capacitors
002436	1	39pF 160V Polystyrene Capacitor
002611	2	1200pF 160V Polystyrene Capacitor
002191	1	0.033μF 250V Polyester Capacitor
002212	1	0.068μF 100V Polyester Capacitor
002261	1	0.47μF 100V Polyester Capacitor
002114	1	6.4μF 25V Electrolytic Capacitor
		Resistors (5% ½W Carbon Film)
000560	1	10Ω
001043	3	1K0
001085	2	1K5
001204	1	4K7
001281	1	10K
001372	1	24K
001386	2	27K
		Transistors & Diodes
002793	2	BC108 Transistors
002912	1	1N914 Diode

CHARACTER GENERATOR

Part No.	Qty	Description
		Miscellaneous
008246	1	PCB Ready for assy
007714	1	Handle, with test points
006664	2	Bus Bar
003045	69	Pin, solder
007525	12	Transistor mounting Pads, T018
008295	2	Mounting Pad – 8 pin DIL
008134	1	IC Socket Mounting Pad, 16 pin DIL
007532	1	Transistor Mounting Pad, T05
		Integrated Circuits
003514	2	SN7400N
007035	1	SN7432N
003612	1	SN7486N
003633	2	SN7493AN
003640	1	SN74121N
008344	1	SN74387N
003682	1	SN15836N
005320	4	SN74151N
008183	2	LM310H
		Capacitors
002562	1	470pF, 160V, Polystyrene
002604	2	1000pF, 160V, Polystyrene
002646	1	2200pF, 160V, Polystyrene
002660	1	3300pF, 160V, Polystyrene
002961	1	0.01μF, 100V, Polyester
002226	1	0.1μF,100V, Polyester
002254	1	0.33μF, 100V, Polyester
002261	3	0.47μF, 100V, Polyester
		Potentiometers
006923	4	100Ω, Cermet, multiturn
		Transistors & Diodes
002793	2	BC108
002842	5	BCY70
002814	1	BFY50
002870	5	BSX20
002912	3	1N914
005705	2	BZY88 – C5V1
		Resistors (0.5W, carbon film, 5%)
000861	2	180Ω
000875	4	200Ω
000882	1	220Ω
000903	2	270Ω
000952	1	430Ω
001001	1	680Ω
001015	2	750Ω
001022	2	820Ω
001036	1	910Ω
001043	10	1K
001064	1	1K2
001120	4	2K2
001162	6	3K3
001183	1	3K9
001225	2	5K6
001421	1	39K
001141	2	2K7
002926	2	Diode, 0A47
002205	1	Capacitor, 0.047μF 100V Polyester

INTERRUPTED RAMP GENERATOR

Part No.	Qty.	Description
		Miscellaneous
008232	1	P C B ready for assy
006664	2	Bus Bar
007714	1	Handle with Test Points
003045	23	Pin, Solder
007525	5	Transistor Mounting Pad
008295	3	Mounting Pad, 8 pin DIL.
		Integrated Circuits
003514	1	SN7400N
003633	4	SN7493AN
007126	2	SN74175N
008183	1	LM310H
008190	2	LM318H
008281	1	MC1408
003682	2	SN15836N
		Capacitors
002366	1	10pF, 160V, Polystyrene, 5%
002471	1	82pF, 160V, Polystyrene, 5%
002590	1	820pF, 160V, Polystyrene, 5%
002604	2	1000pF, 160V, Polystyrene, 5%
006293	1	0.047μF, Ceramic, 25V
002163	1	0.01μF, Polyester, 250V
002205	1	0.047μF, Polyester, 250V
002261	3	0.47μF, Polyester, 100V
002282	1	1μF, Polyester, 100V
		Transistors & Diodes
002793	2	BC108
002800	2	BC109
002842	2	BCY70
002870	1	BSX20
002912	4	1N914
005705	2	BZY88 – C5V1
005740	2	BZY88 – C7V5
		Resistors (5%, ½W, Carbon Film)
000924	1	330Ω
001043	4	1K
001113	1	2K
001141	1	2K7
001162	3	3K3
001204	2	4K7
001225	2	5K6
001253	1	7K5
001281	4	10K
001365	2	22K
001526	1	100K
001603	1	220K
002926	2	0A47 Diode
002520	1	220pF Capacitor, 160V, Polystyrene
001211	1	5K1Ω Resistor
001323	1	15K Resistor
001085	1	1K5 Resistor
001022	1	820Ω Resistor

FORMATTER

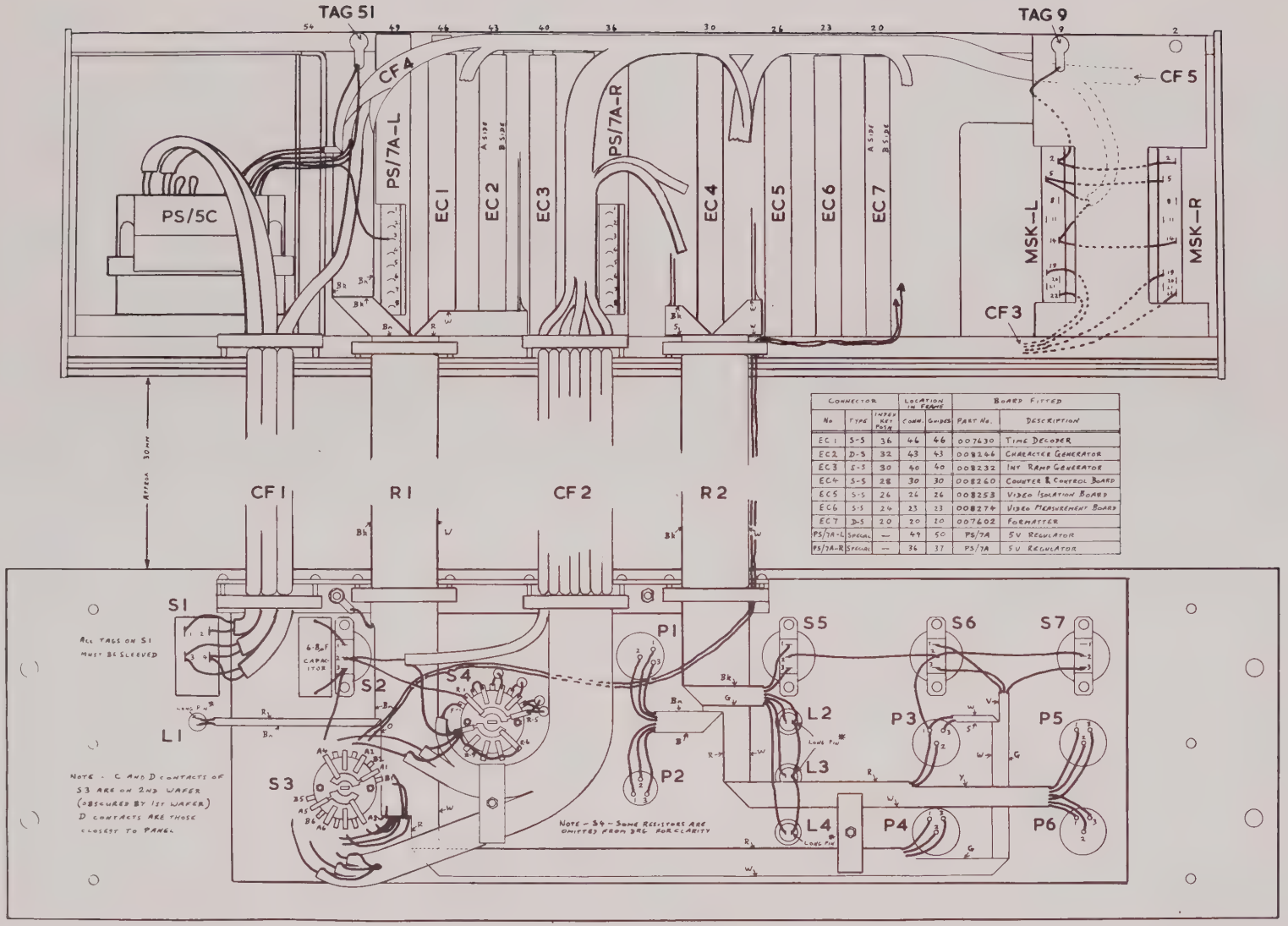
Part No.	Qty.	Description
		Miscellaneous
007602	1	P.C. Board, ready for assembly
003045	168	Pin, solder
006664	4	Bus Bar
007714	1	Handle, with test points
008134	1	IC socket, 16-pin
003360	1	Potentiometer, cermet, 5 KΩ
		Integrated Circuits
003514	2	SN7400N
003535	1	SN7404N
006972	1	SN7408N
007035	1	SN7432N
006251	1	SN7433N
003570	1	SN7442AN
003591	1	SN7474N
003626	1	SN7490AN
007791	1	SN74107N
006986	1	SN74123N
005873	4	SN74150N
005320	1	SN74151AN
008106	1	SN74S158N
008113	1	SN74177N
008120	1	SN74188AN (To be fitted on test)
007896	1	MC4024P
		Diodes
002926	1	0A47
		Capacitors
002506	1	150pF, 5%, 160V, Polystyrene
002520	2	220pF, 5%, 160V, Polystyrene
002583	1	680pF, 5%, 160V, Polystyrene
002646	4	2200pF, 5%, 160V, Polystyrene
002226	2	0.1μF, 10%, 100V, Polyester
002240	1	0.22μF, 10%, 100V, Polyester
002261	1	0.47μF, 10%, 100V, Polyester
002282	1	1.0μF, 10%, 100V, Polyester
002296	1	1.5μF, 10%, 100V, Polyester
		Resistors (all 5%, ½W, carbon film)
000903	2	270Ω
000994	7	620Ω
001043	1	1K0
001113	1	2K0
001120	4	2K2
001134	1	2K4
001155	1	3K0
001225	9	5K6
001253	1	7K5
001302	1	12K
001386	2	27K

TYPE PS/5C UNREGULATED POWER SUPPLY

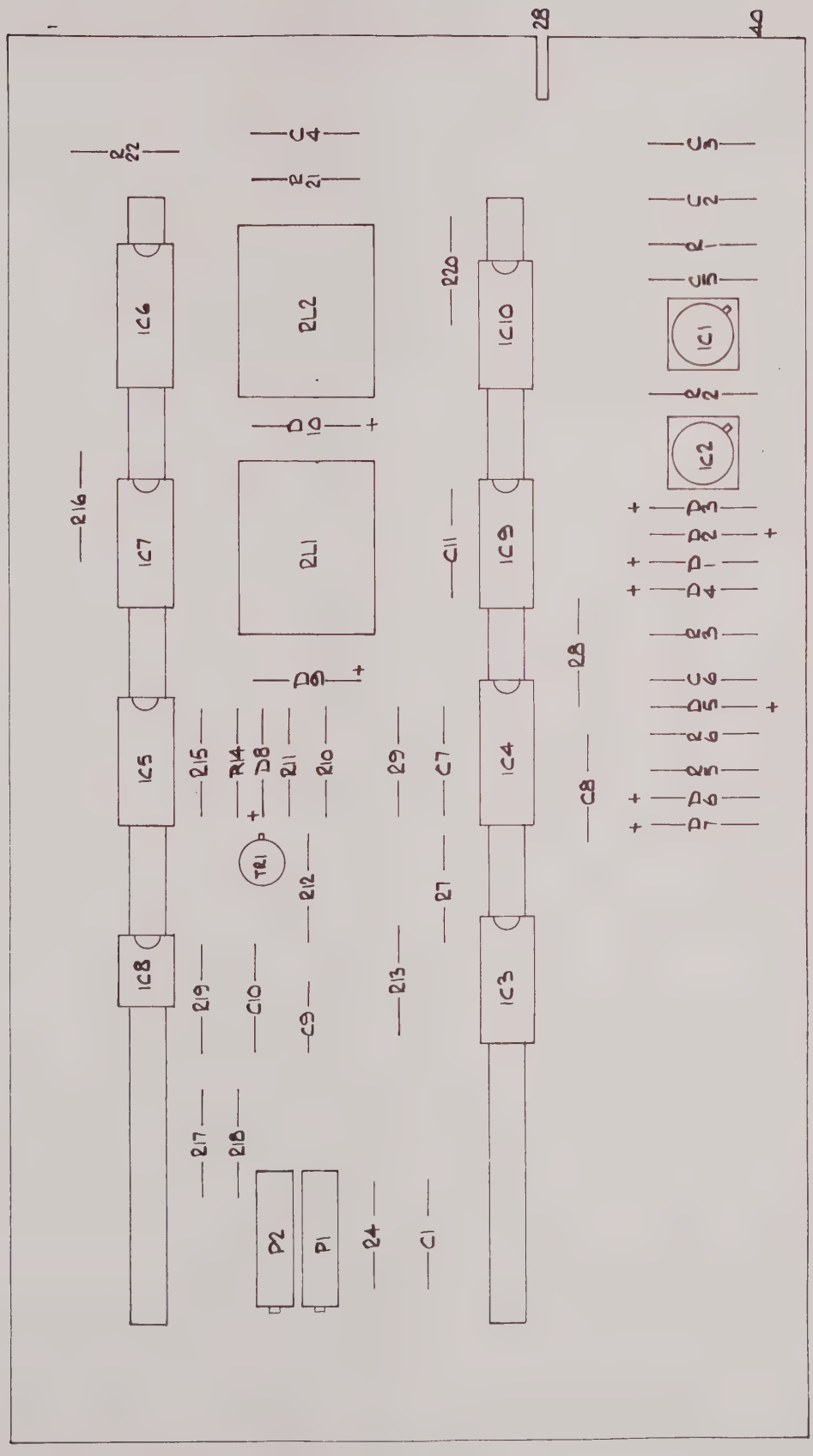
Part No.	Qty.	Description
	1	Mounting Plate
	1	Screening Plate
	1	Front Bracket
	1	Base Bracket
	1	Rear Bracket
	1	Mains Cover
006776	1	Transformer, mains
006615	1	Capacitor, electrolytic, 22000μF, 16V
006622	1	Clamp, capacitor
006783	1	Rectifier, bridge, BR-101A
006755	3	Fuseholder, open (20 x 5mm)
003311	3	Fuse, 20 x 5mm, 3A
003234	1	Fuseholder, enclosed (20 x 5mm)
003304	1	Fuse, 20 x 5mm, 2A
005131	1	Plug, 3-pin, mains
006790	1	Suppressor, interference, mains
007203	3	Tag, stand-off PTFE
006811	1	Connector block, 24-way, male
006825	14	Contact, crimp type (socket)
003185	1	Tag, solder, 6BA
003164	2	Tag, solder, 2BA
007196	2	Nut sert, M3
004613	10	Screw, pan head, M3 x 6
004641	2	Screw, pan head, M3 x 16
004774	9	Screw, CSK head, M3 x 8
004795	2	Screw, CSK head, M3 x 16
004662	2	Screw, pan head, M4 x 8
004683	1	Screw, pan head, M4 x 16
004893	21	Nut, M3
004900	7	Nut, M4
004991	21	Washer, shakeproof, M3
005005	7	Washer, shakeproof, M4
	30cm	Wire, 16/0.2, Blue
004823	4	Screw, CSK head, M4 x 12
	50cm	Wire, 16/0.2, red
	30cm	Wire, 16/0.2, black
	30cm	Wire, 16/0.2, orange
	30cm	Wire, 16/0.2, yellow
	30cm	Wire, twin, "oval mains"
	1	Foam rubber (or similar) block
	–	Adhesive, Clear Bostik or similar
	1	Resistor, 330Ω

PS/7A – REGULATOR UNIT

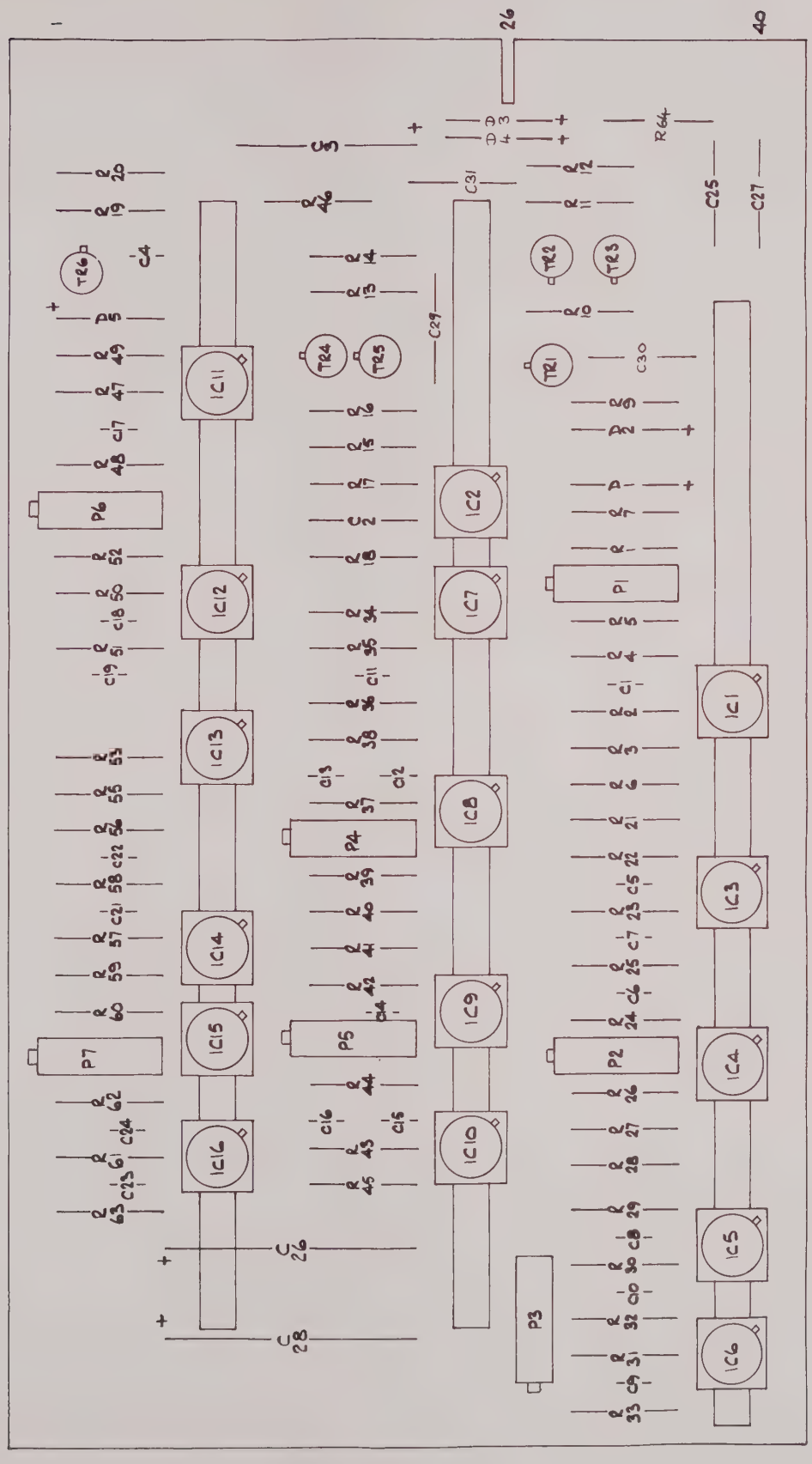
Part No.	Qty.	Description
007420	1	Heat Sink
007434	1	Spacer
007413	1	Voltage Regulator I C. LM323K
002051	2	Capacitor, Electrolytic, 4.7μF, 63V
004662	2	Screw, M4 x 8, Pan head
004900	2	Nut, M4
005005	4	Washer, S/p, M4
003171	1	Solder tag, 4BA
007441	1	Plug, 8-way, ("strip connector")
004634	2	Screw, M3 x 12, Pan head
004893	2	Nut, M3
004991	4	Washer, S/p, M3
	25cm	Wire, tinned copper, 20swg
	20cm	Sleeving, silicone rubber
		Silicone grease



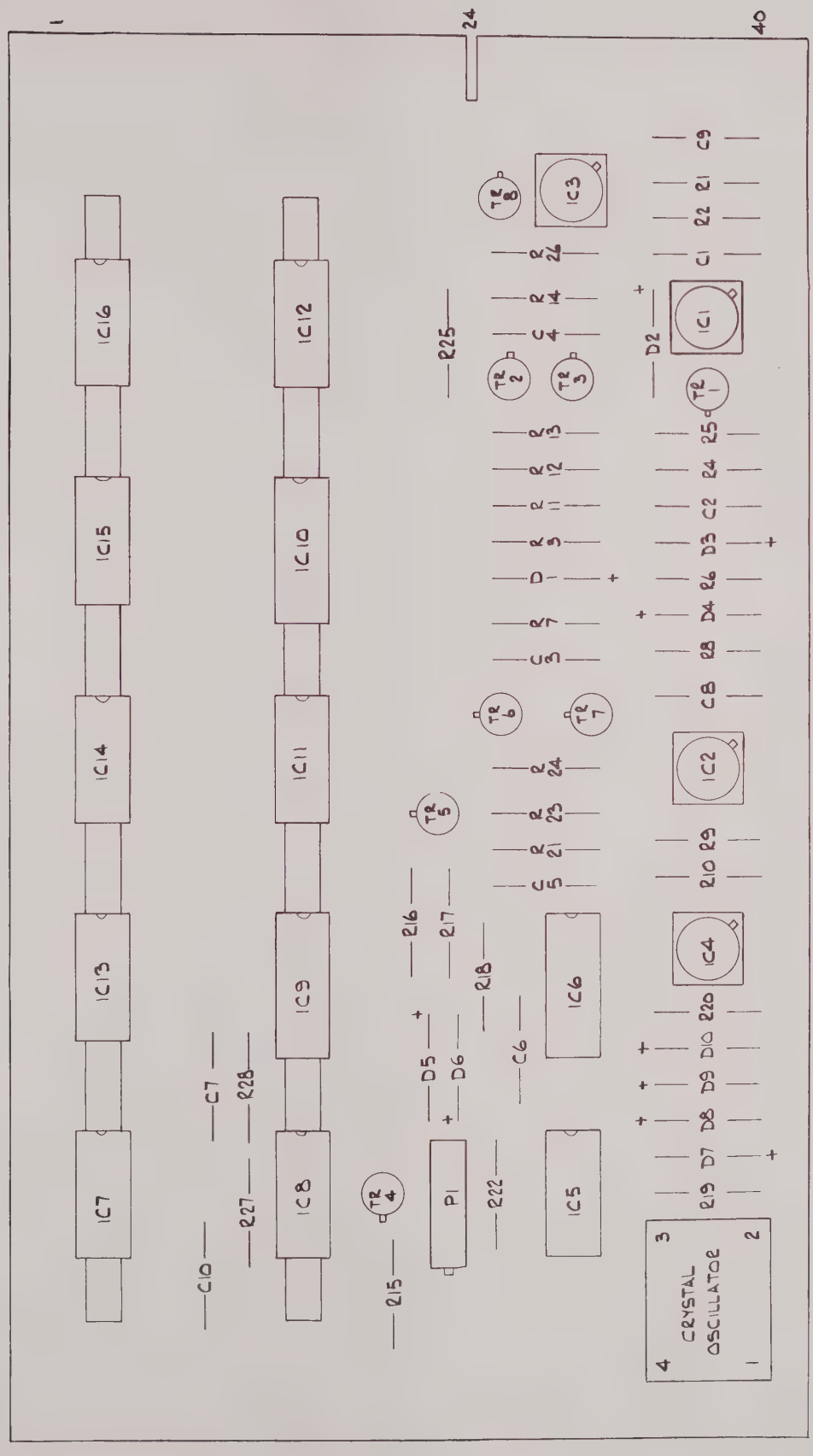
CONNECTOR			LOCATION IN FRAME		BOARD FITTED	
No	TYPE	INDEX KEY POS'N	COMP.	GUIDES	PART No.	DESCRIPTION
EC 1	S-S	36	46	46	007630	TIME DECODER
EC2	D-S	32	43	43	008246	CHARACTER GENERATOR
EC3	S-S	30	40	40	008232	INT RAMP GENERATOR
EC4	S-S	28	30	30	008260	COUNTER & CONTROL BOARD
EC5	S-S	26	24	26	008253	VIDEO ISOLATION BOARD
EC6	S-S	24	23	23	008274	VIDEO MEASUREMENT BOARD
EC7	D-S	20	20	20	007602	FORMATTER
PS/7A-L	SPECIAL	—	49	50	PS/7A	5V REGULATOR
PS/7A-R	SPECIAL	—	36	37	PS/7A	5V REGULATOR



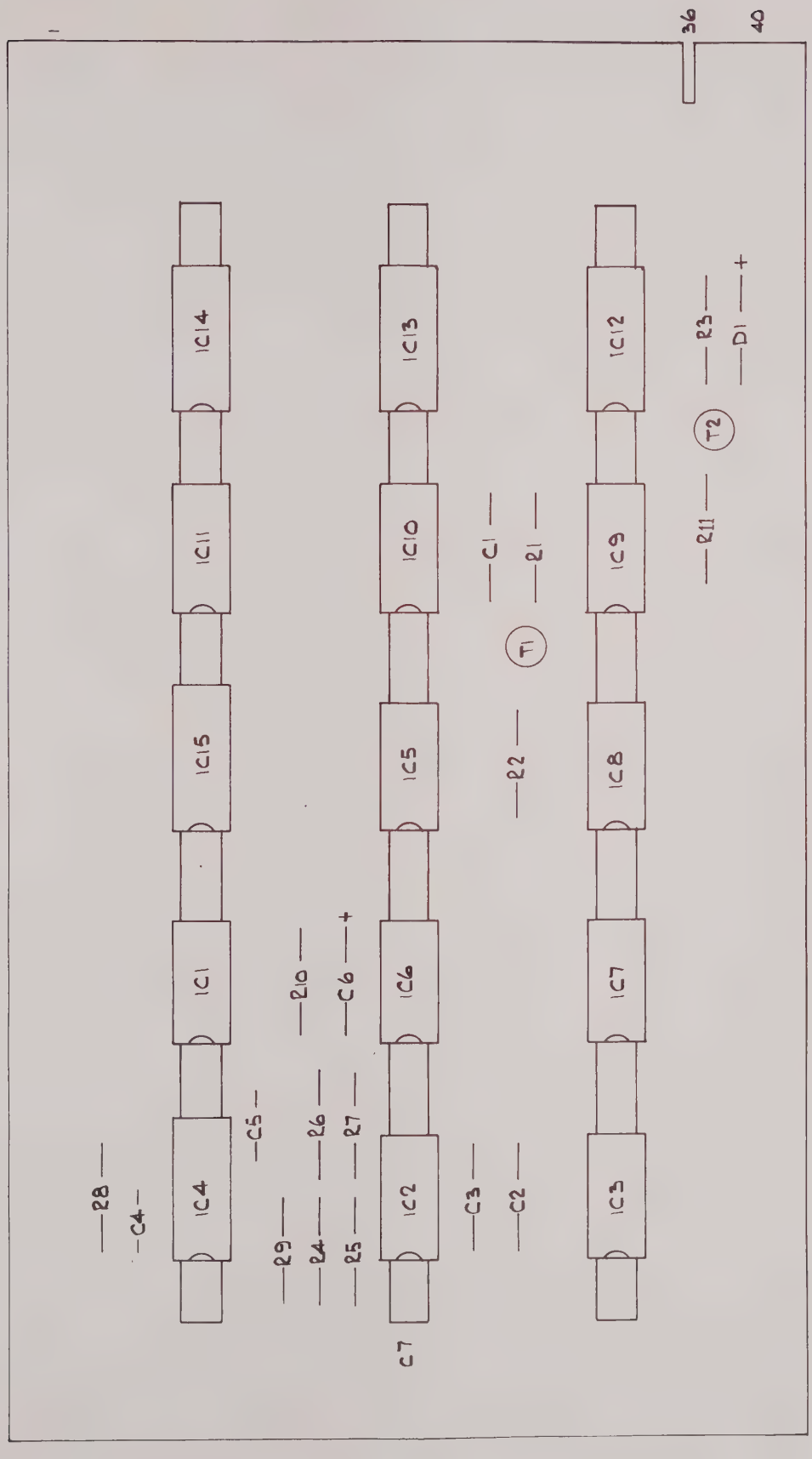
GSDA/1 – COUNTER & CONTROL P.C.B. – COMPONENT LOCATION



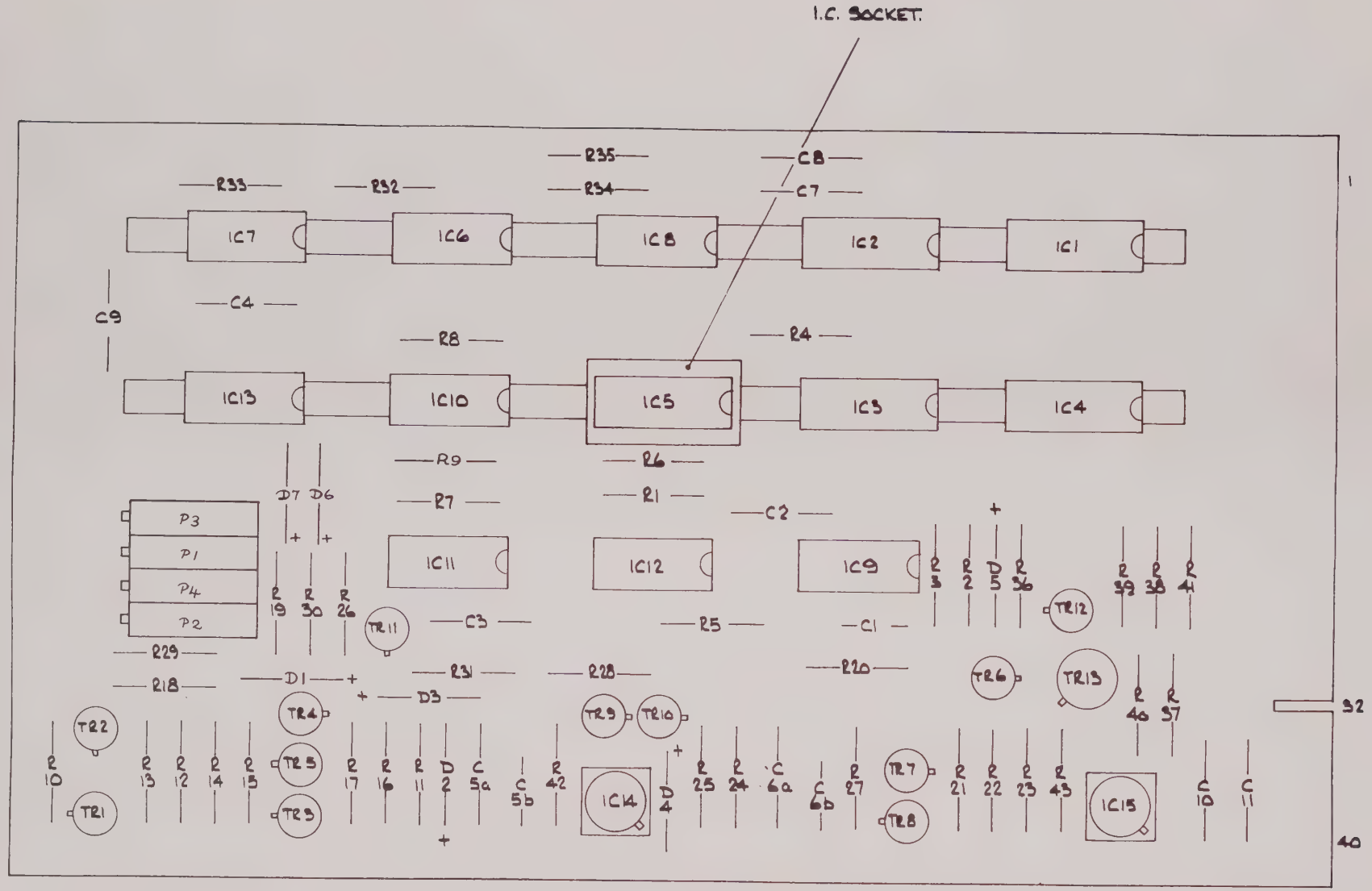
GSDA/1 – VIDEO ISOLATOR P.C.B. – COMPONENT LOCATION

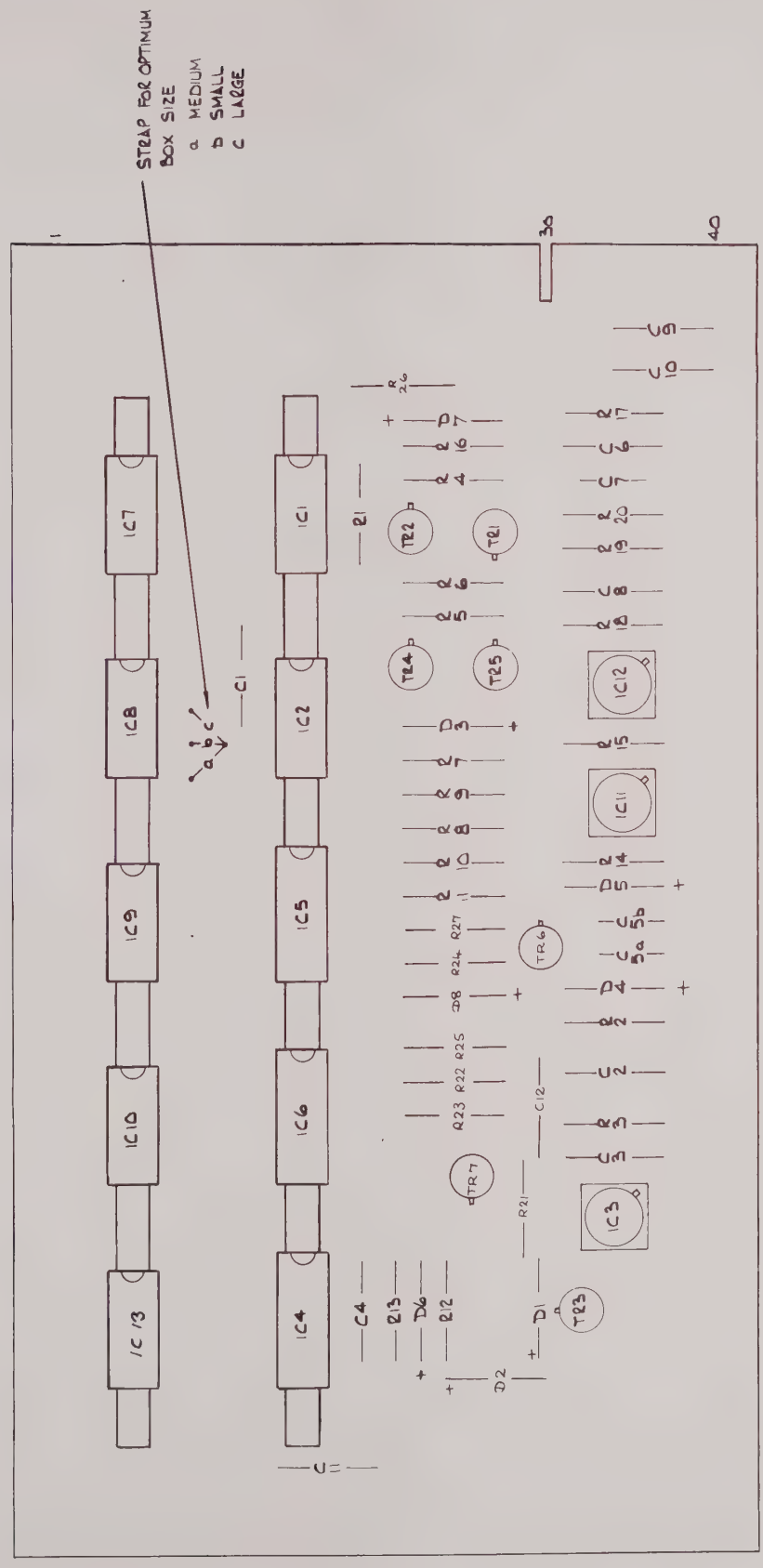


GSDA/1 – VIDEO MEASUREMENT P.C.B. COMPONENT LOCATION

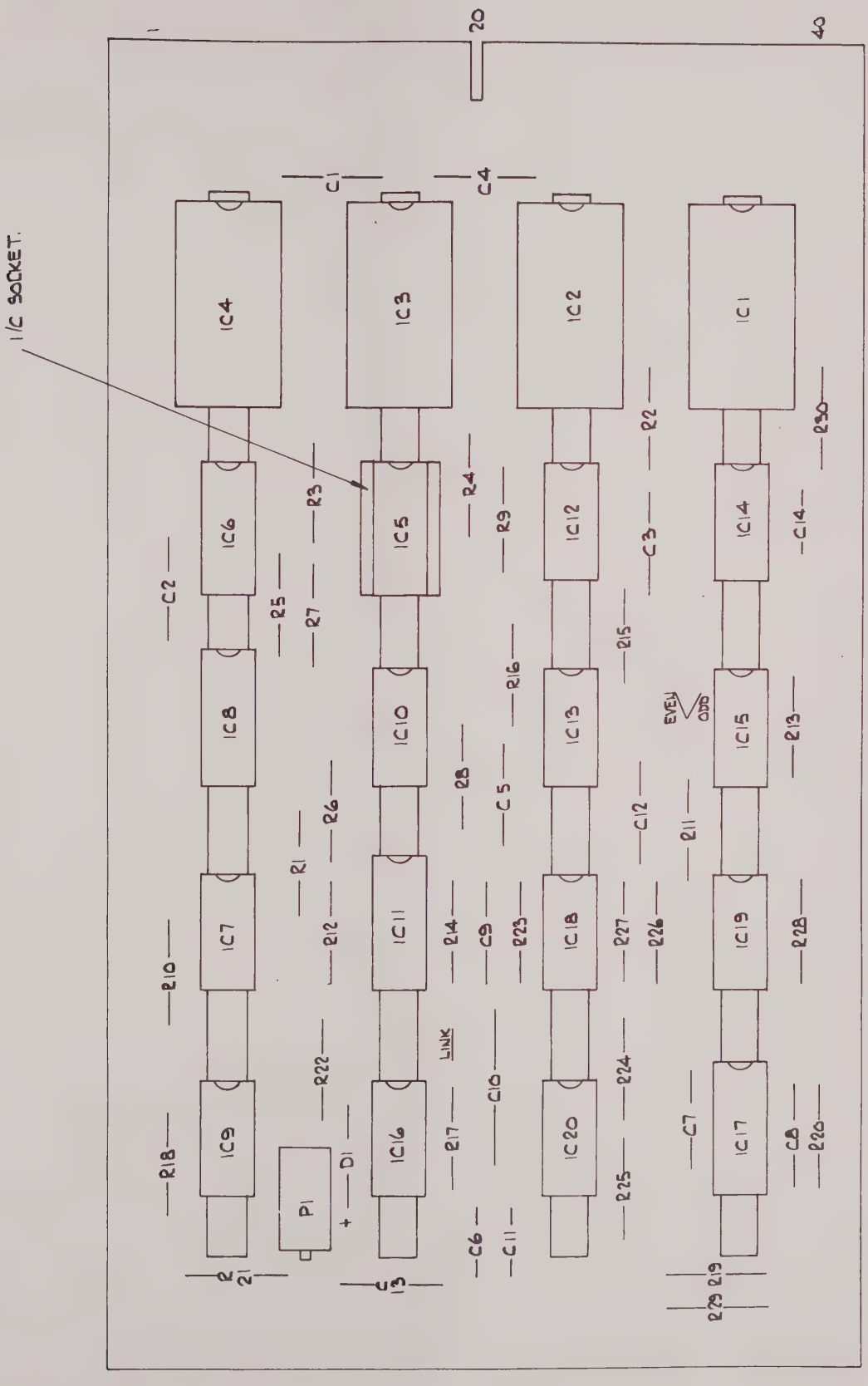


GSDA/1 – TIME DECODER P.C.B. COMPONENT LOCATION


I.C. SOCKET.
R35
C8
R33
R32
R34
C7
IC7
IC6
IC8
IC2
IC1
C9
C4
R8
R4
IC13
IC10
IC5
IC3
IC4
R9
R6
D7
D6
R7
R1
C2
P3
P1
P4
P2
IC11
IC12
IC9
R19
R30
R26
TR11
C3
R5
C1
TR12
R29
R18
D1
R31
R28
R20
TR6
TR13
D3
TR4
TR9
TR10
TR2
TR5
TR1
TR3
IC14
D4
IC15
TR7
TR8
C10
C11
1
32
40



GSDA/1 – INTERRUPTED RAMP GENERATOR – COMPONENT LOCATION



GSDA/1 – FORMATTER P.C.B. COMPONENT LOCATION

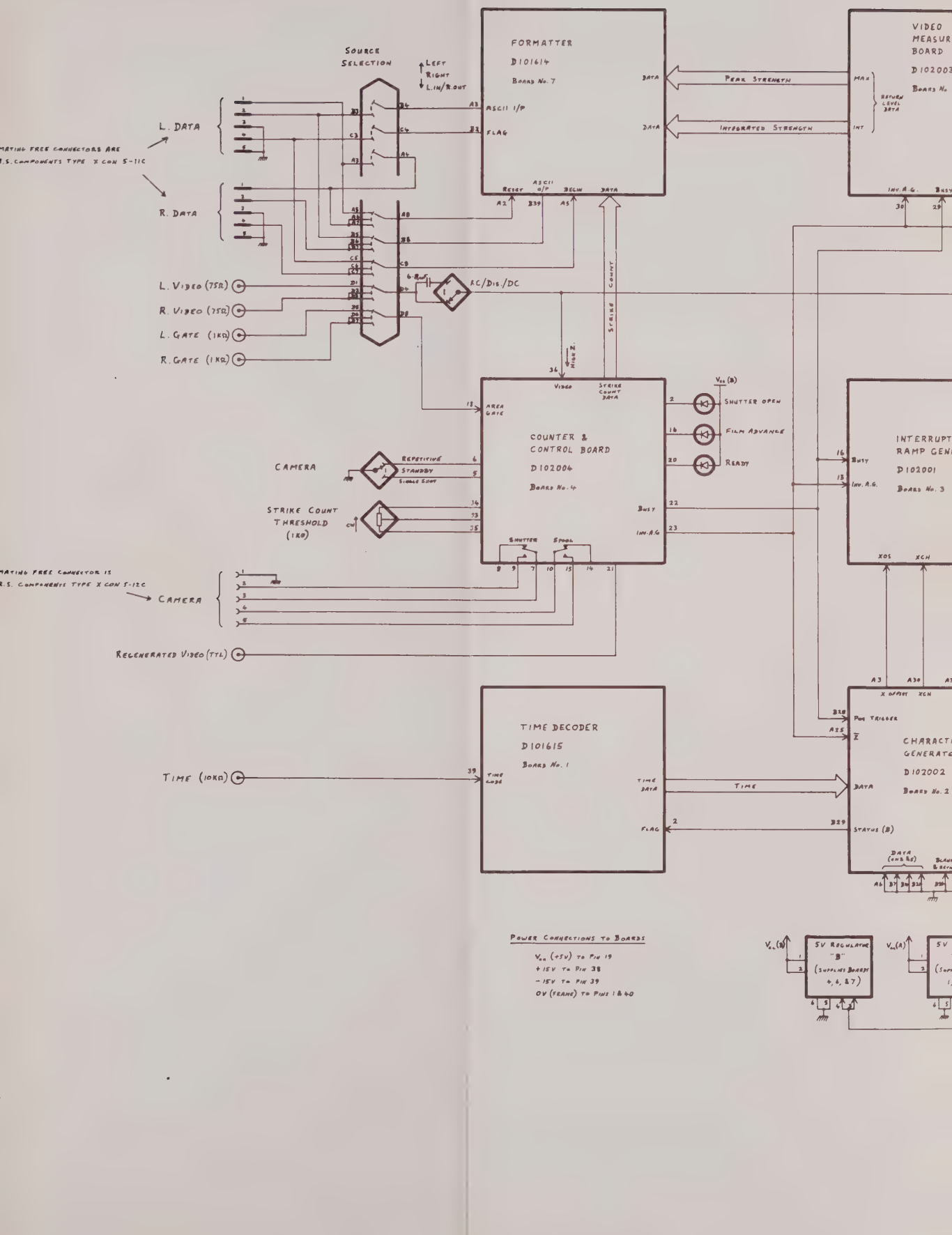
WIRING SCHEDULE

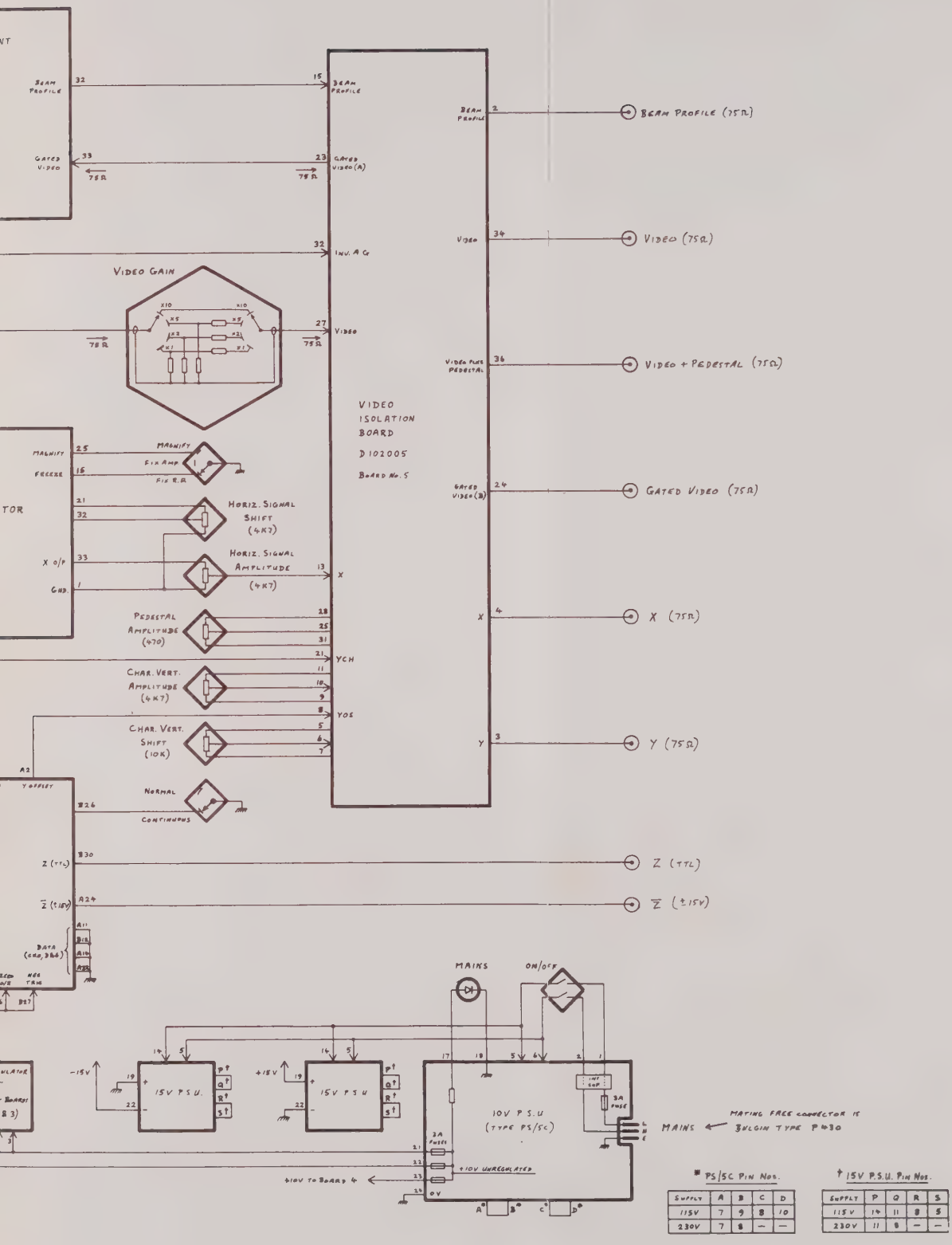
FROM		ROUTE	TO	
UNIT	TAG		UNIT	TAG
EC1,2,3,4,5,6,7	1.40	Rectangle 4" x 8"	Frame	51
0V Bus		Vert. link between EC4, EC5	0V Bus	
PS/5C	24	Direct	Frame	51
PS/7A-L	5,6	Direct	0V Bus	
PS/7A-R	5,6	Direct	0V Bus	
MSK-L	22	CF3	EC7	40
MSK-R	19	CF3	EC7	40
MSK-R	22	CF3	EC2,3,4,5 & 6	39
MSK-L	19	CF3	EC2,3,4,5 & 6	38
PS/7A-L	1,2	Direct	EC2 (A,B) EC1, EC3	19
PS/7A-R	1,2	Direct	EC4, EC6, EC7 (A,B)	19
PS/5C	21	Direct	PS/7A-L	3,4
PS/5C	22	CF4	PS/7A-R	3,4
PS/5C	23	CF4	EC4	17
PS/5C	1	CF1	S1	1
	2			2
PS/5C	5	CF1	S1	3
	6			4
S1	3	CF1, CF4	MSK-L	14
	4			5
MSK-L	14	Direct	MSK-R	14
MSK-L	5	Direct	MSK-R	5
MSK-L	2	Direct	MSK-R	2
MSK-L	2	Direct	Frame	9
PS/5C	7	1" of wire	PS/5C	8
PS/5C	11	1" of wire	PS/5C	12
Fr. Panel	Earth tag	R1, CF4	Frame	51
L1	Long pin	R1, CF4	PS/5C	18
L1	Short pin	R1, CF4	PS/5C	17
S3-A	8	R1, CF4	EC7	A2
S3-B	8	R1, CF4	EC7	B39
S3-C	8	R1, CF4	EC7	A5
S3-A	3,5	R1, CF4, CF5	L. Data Skt	1
S3-B	3,5	R1, CF4, CF5	L. Data Skt	2
S3-C	3,5	R1, CF4, CF5	L. Data Skt	4
S3-A	4,6,7	R1, CF4, CF5	R. Data Skt	1
S3-B	6,7	R1, CF4, CF5	R. Data Skt	2
S3-C	6,7	R1, CF4, CF5	R. Data Skt	4
P4	1	R1	EC3	1
P4	2	R1	EC3	32
P4	3	R1	EC3	21
S7	3	R1	EC2	B26
S6	3	R1	EC3	15
S6	1	R1	EC3	25
P3	3	R1	EC3	33
P3	1	R1	EC3	1
P3	1	Direct	S7, S6, S5	2
S2	2	CF2	EC4	36
S4-R	10			40
S4-F	1	CF2	EC5	27
S4-R	10			30
S3-D	2,3	CF2, CF5	R. Video Skt	Pin
S4-R	10			Tag
S3-D	1	CF2, CF5	L. Video Skt	Pin
S4-R	10			Tag
S3-D	6,7	CF2, CF5	R. Gate Skt	Pin
Join to 50 & 51				Tag

FROM		ROUTE	TO	
UNIT	TAG		UNIT	TAG
S3-D Join to 49 & 51	8	CF2	EC4	18 40
S3-D Join to 49 & 50	5	CF2, CF5	L.Gate Skt	Pin Tag
S2	2	Direct	S4-R	1
S2	3	Direct	S3-D	4
S2	1	Direct	S2	3
S4-F	2	Direct	S4-R	2
S4-F	3	Direct	S4-R	3
S4-F	4	Direct	S4-R	4
S4-F	5	Direct	S4-R	5
S4-R	3	Direct	S4-R	8
S4-R	4	Direct	S4-R	7
S4-R	5	Direct	S4-R	6
S4-R	10	Direct	S4-R	9,8,7,6
S5	1	R2	EC4	6
S5	3	R2	EC4	5
L2,3,4	Short Pin	R2	EC4	19
L2	Long Pin	R2	EC4	20
L3	Long Pin	R2	EC4	16
L4	Long Pin	R2	EC4	2
P2	3	R2	EC4	34
P2	2	R2	EC4	33
P2	1	R2	EC4	35
P1	2	R2	EC5	25
P1	1	R2	EC5	31
P1	3	R2	EC5	28
P3	1	R2	EC5	0V Bus
P3	2	R2	EC5	13
P5	1	R2	EC5	9
P5	2	R2	EC5	10
P6	3	R2	EC5	7
P5	3	R2	EC5	11
P6	2	R2	EC5	6
P6	1	R2	EC5	5
EC1	39 40	CF5	Time Skt	Pin Tag
EC1	37	Direct	EC2	A23
EC1	34	Direct	EC2	A20
EC1	32	Direct	EC2	A12
EC1	26	Direct	EC2	B23
EC1	25	Direct	EC2	B22
EC1	24	Direct	EC2	B20
EC1	23	Direct	EC2	B15
EC1	22	Direct	EC2	B13
EC1	16	Direct	EC2	B11
EC1	15	Direct	EC2	B10
EC1	14	Direct	EC2	B8
EC1	13	Direct	EC2	B5
EC1	12	Direct	EC2	B3
EC1	11	Direct	EC2	B2
EC1	8	Direct	EC2	A10
EC1	7	Direct	EC2	A9
EC1	6	Direct	EC2	A8
EC1	5	Direct	EC2	A7
EC1	4	Direct	EC2	A5
EC1	3	Direct	EC2	A4
EC1	2	Direct	EC2	B29
EC2	B1	Direct	EC2	A6. B6, B7
EC2	A6. B6, B7	Direct	EC2	A11. B12.

FROM		ROUTE	TO	
UNIT	TAG		UNIT	TAG
EC2	A11. B12.	Direct	EC2	A14. B14.
EC2	A14. B14.	Direct	EC2	B21. A22.
EC2	A22. B21.	Direct	EC2	B24.
EC2	B24	Direct	EC2	B27
EC2	B28	Direct	EC3	16
EC3	16	Direct	EC4	22
EC4	22	Direct	EC6	29
EC2	A31	Direct	EC5	21
EC2	B30 B40	CF5	Z Skt.	Pin Tag
EC2	A24 A40	CF5	$\bar{Z}$ Skt.	Pin Tag
EC2	A30	Direct	EC3	29
EC2	A3	Direct	EC3	31
EC2	A2	Direct	EC5	8
EC2	A25	Direct	EC3	13
EC3	13	Direct	EC4	23
EC4	23	Direct	EC5	32
EC5	32	Direct	EC6	30
EC6	33	Direct	EC5	23
EC6	32	Direct	EC5	15
EC6	28	Direct	EC7	B24
EC6	27	Direct	EC7	B14
EC6	26	Direct	EC7	B6
EC6	25	Direct	EC7	B34
EC6	23	Direct	EC7	B23
EC6	22	Direct	EC7	B5
EC6	21	Direct	EC7	B33
EC6	20	Direct	EC7	B13
EC6	18	Direct	EC7	B28
EC6	17	Direct	EC7	B18
EC6	16	Direct	EC7	B38
EC6	15	Direct	EC7	B27
EC6	14	Direct	EC7	B17
EC6	13	Direct	EC7	B37
EC6	12	Direct	EC7	B26
EC6	11	Direct	EC7	B16
EC6	10	Direct	EC7	B36
EC6	9	Direct	EC7	B25
EC6	8	Direct	EC7	B15
EC6	7	Direct	EC7	B35
EC6	6	Direct	EC7	B10
EC6	5	Direct	EC7	B9
EC6	4	Direct	EC7	B8
EC6	3	Direct	EC7	B7
EC5	2 0V Bus	CF5	Beam Profile Skt	Pin Tag
EC5	3 0V Bus	CF5	Y Skt	Pin Tag
EC5	4 0V Bus	CF5	X Skt	Pin Tag
EC5	24 0V Bus	CF5	Gated Video Skt	Pin Tag
EC5	34 0V Bus	CF5	Video Skt	Pin Tag

FROM		ROUTE	TO	
UNIT	TAG		UNIT	TAG
EC5	36 0V Bus	CF5	V + P Skt	Pin Tag
EC4	15	CF5	Cam. Skt	5
EC4	10	CF5	Cam. Skt	4
EC4	7	CF5	Cam. Skt	3
EC4	9	CF5	Cam. Skt	2
EC4	1	CF5	Cam. Skt	1
EC4	21	CF5	Regen. Video Skt	Pin
EC4	1	CF5	Regen. Video Skt	Tag
EC4	32	Direct	EC7	B22
EC4	31	Direct	EC7	B12
EC4	30	Direct	EC7	B4
EC4	29	Direct	EC7	B21
EC4	27	Direct	EC7	B11
EC4	26	Direct	EC7	B31
EC4	25	Direct	EC7	B32
EC4	24	Direct	EC7	B3
L. Data Skt	3,5.	Direct	R. Data Skt	3,5.
R. Data Skt	3,5.	Direct	Mtg. Brkt. Conn.	Earth tag
S3-B	4	Alongside R2	EC7	A3
S3-C	4	Alongside R2	EC7	B2

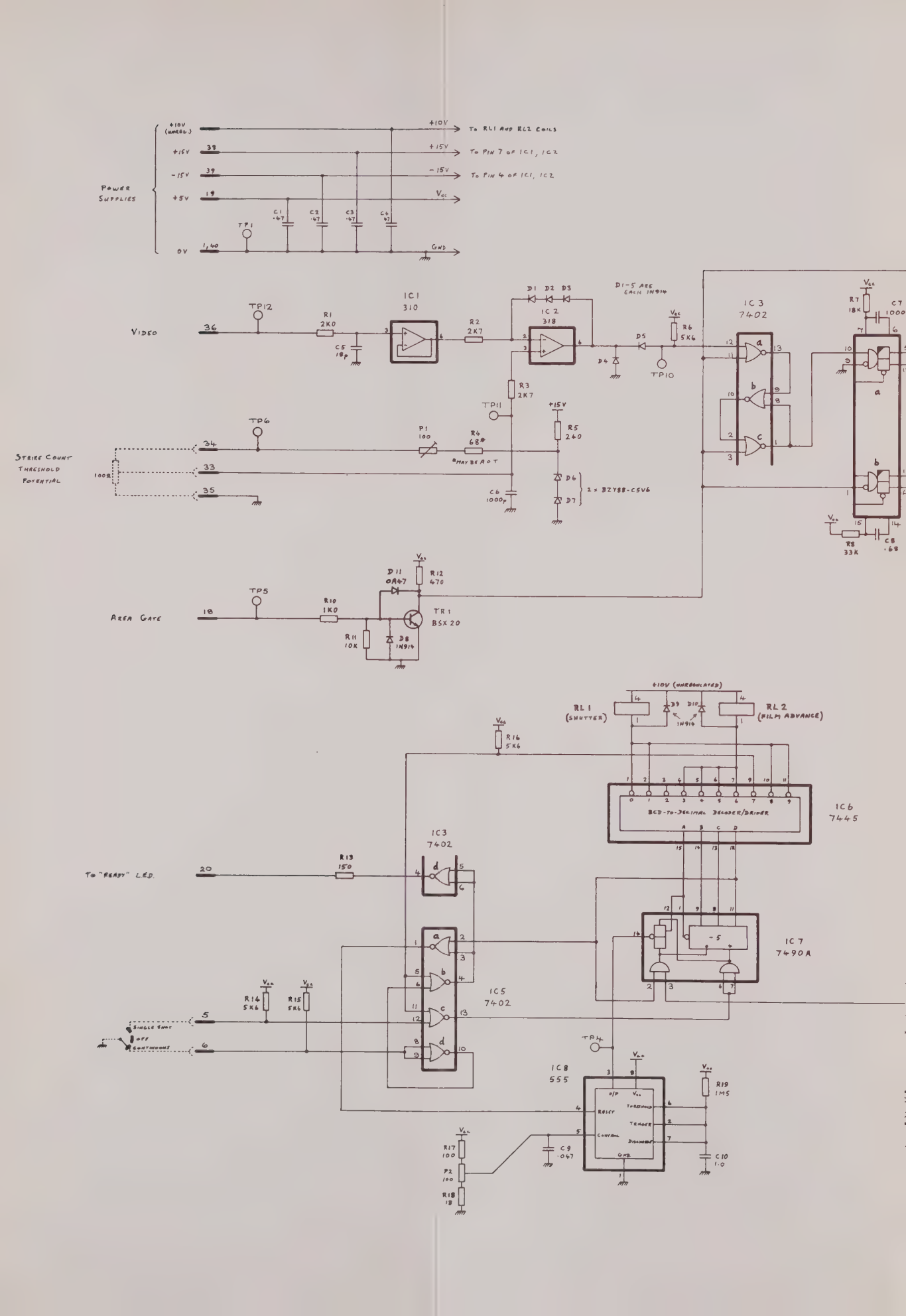

FORMATTER
D101614
BOARD No. 7
ASCII I/P
FLAG
DATA
DATA
PEAK STRENGTH
INTEGRATED STRENGTH
VIDEO MEASUR BOARD
D102003
BOARD No.
MAX
INT
RETURN LEVEL DATA
SOURCE SELECTION
LEFT
RIGHT
L.IN/R.OUT
L. DATA
R. DATA
MATING FREE CONNECTORS ARE R.S. COMPONENTS TYPE X CON 5-11C
L. VIDEO (75Ω)
R. VIDEO (75Ω)
L. GATE (1KΩ)
R. GATE (1KΩ)
RC/DIS./DC
COUNTER & CONTROL BOARD
D102004
BOARD No. 4
AREA GATE
VIDEO
STRIKE COUNT DATA
SHUTTER OPEN
FILM ADVANCE
READY
BUSY
INV. A.G.
CAMERA
REPETITIVE
STANDBY
SINGLE SHOT
STRIKE COUNT THRESHOLD (1KΩ)
SHUTTER
SPOOL
INTERRUPT RAMP GEN
D102001
BOARD No. 3
MATING FREE CONNECTOR IS R.S. COMPONENTS TYPE X CON 5-12C
CAMERA
REGENERATED VIDEO (TTL)
TIME DECODER
D101615
BOARD No. 1
TIME (10KΩ)
TIME CODE
TIME DATA
TIME
FLAG
CHARACTER GENERATO
D102002
BOARD No. 2
DATA
STATUS (B)
POWER CONNECTIONS TO BOARDS
+5V (+5V) TO PIN 19
+15V TO PIN 38
−15V TO PIN 39
0V (FRAME) TO PINS 1 & 40
5V REGULATOR "B"
(SUPPLIES BOARDS 4, 6, & 7)

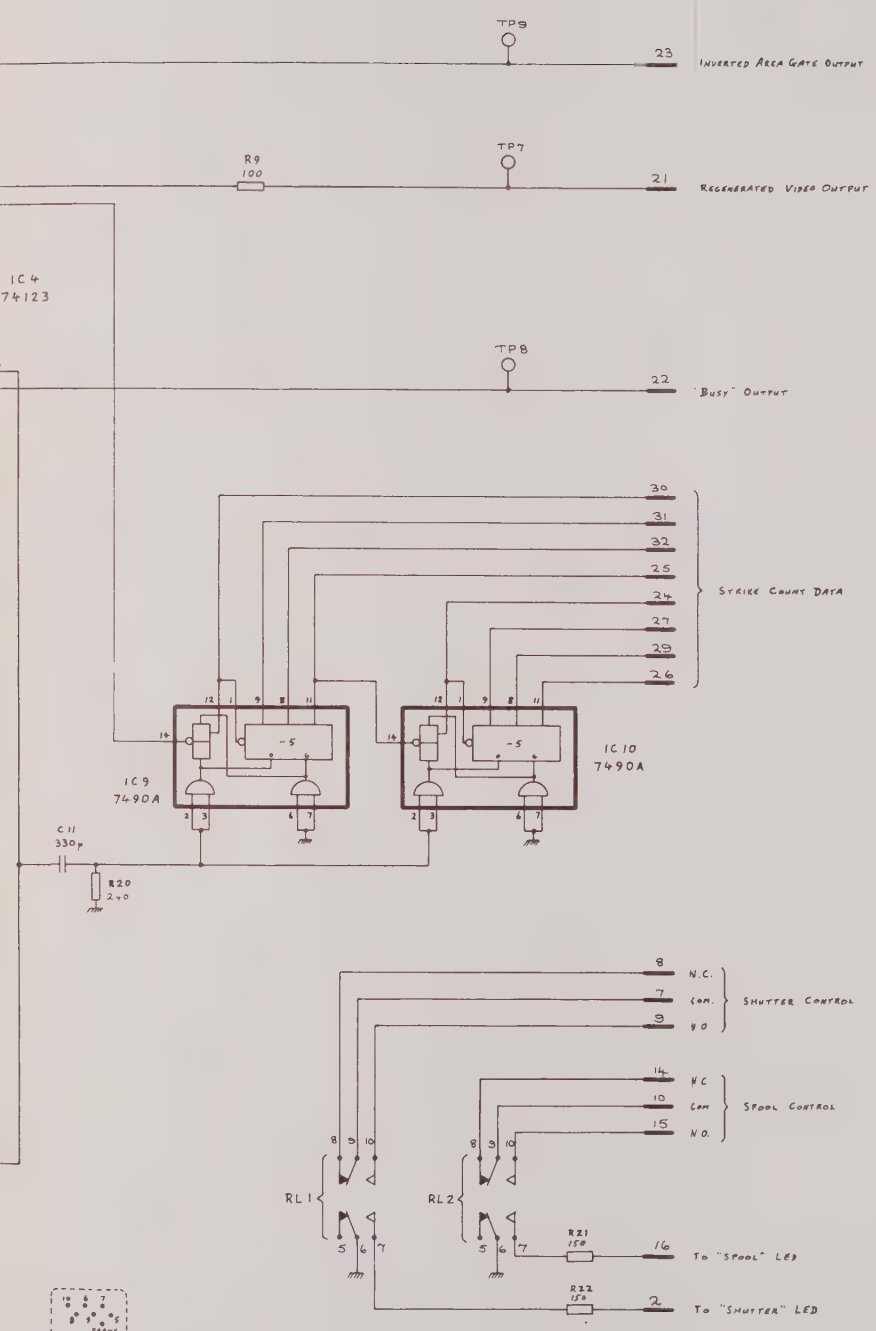


SUPPLY	A	B	C	D
115V	7	9	8	10
230V	7	8	—	—

SUPPLY	P	Q	R	S
115V	14	11	8	5
230V	11	8	—	—

GSDA/1 – SYSTEM DIAGRAM


POWER SUPPLIES
+10V (UNREGD.)
+15V
-15V
+5V
0V
TP1
C1 .47
C2 .47
C3 .47
C4 .47
+10V
+15V
-15V
V_{cc}
GND
To RL1 and RL2 Coils
To Pin 7 of IC1, IC2
To Pin 4 of IC1, IC2
VIDEO
TP12
R1 2K0
C5 18p
IC1 310
R2 2K7
IC2 318
D1 D2 D3
D1-5 ARE EACH IN914
D4
D5
R6 5K6
TP10
R3 2K7
TP11
+15V
R5 240
P1 100
R4 68Ω
MAY BE NOT
TP6
STRIKE COUNT THRESHOLD POTENTIAL
100Ω
D6
D7
2 x BZY88-C5V6
C6 1000p
IC3 7402
R7 18K
C7 1000
C8 .68
R8 33K
AREA GATE
TP5
R10 1K0
D11 OA47
R12 470
TR1 BSX 20
R11 10K
D8 IN914
+10V (UNREGULATED)
RL1 (SHUTTER)
RL2 (FILM ADVANCE)
D9 D10 IN914
R16 5K6
IC6 7445
BCD-TO-DECIMAL DECODER/DRIVER
IC7 7490A
TO "READY" LED.
R13 150
IC5 7402
R14 5K6
R15 5K6
SINGLE SHOT
OFF
CONTINUOUS
TP4
IC8 555
R17 100
P2 100
R18 1Ω
C9 .047
R19 1M5
C10 1.0

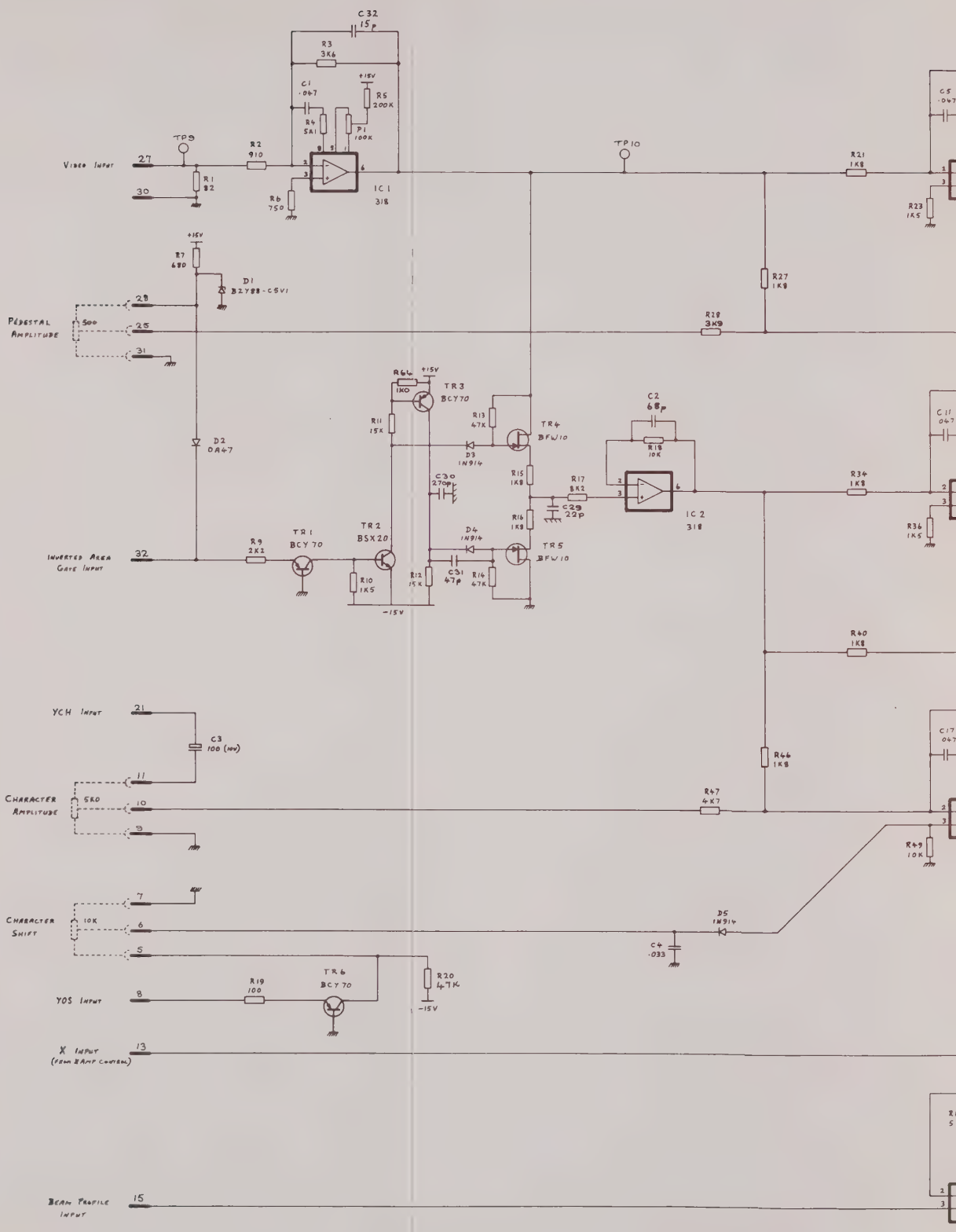


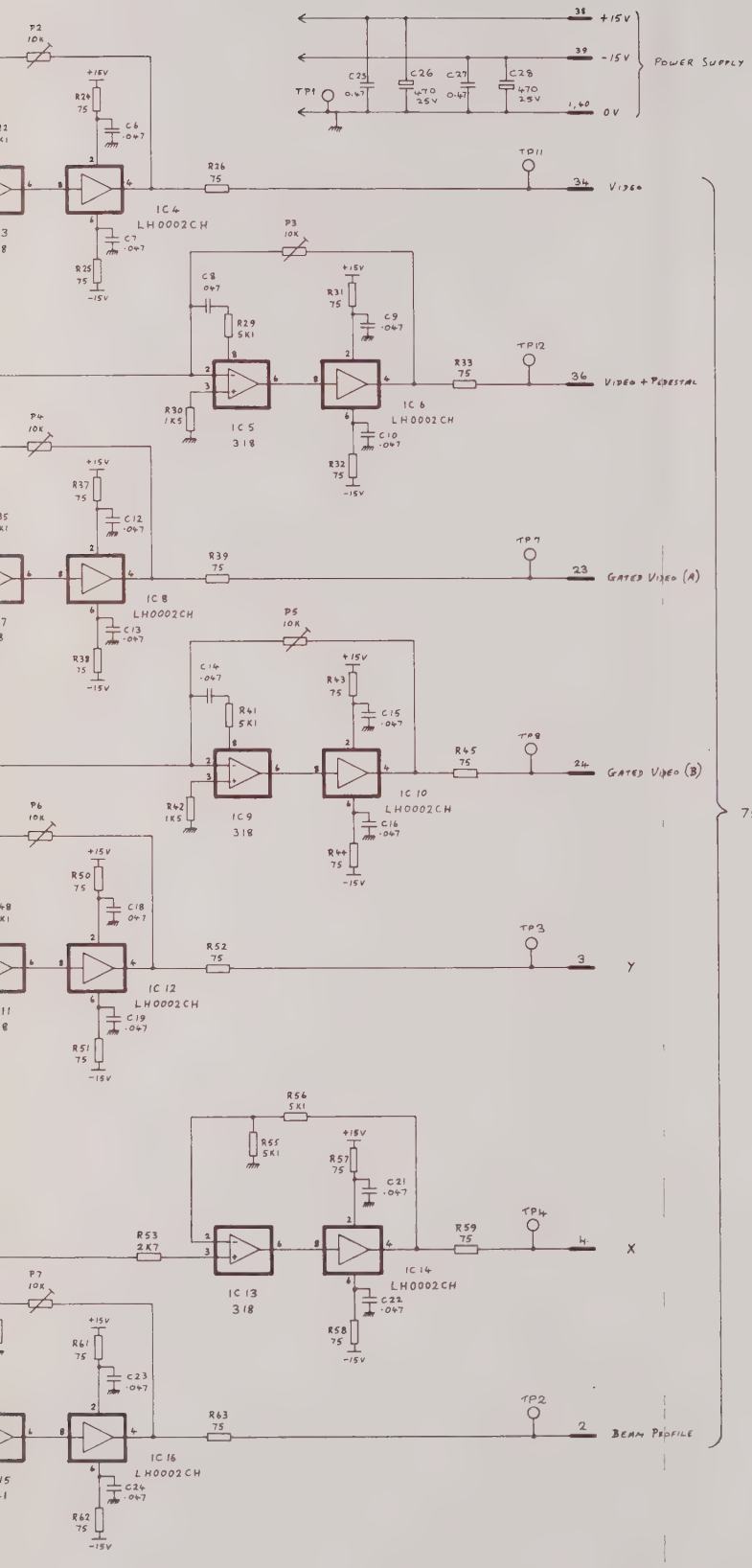
PCB IS PART NO. 003260

INDEX SLOT NO 28

POSITION 4

GSDA/1 – COUNTER & CONTROL BOARD


C32 15p
R3 3K6
C1 .047
+15V
R5 200K
R4 5K1
P1 100K
TP9
R2 910
VIDEO INPUT
27
30
R1 82
R6 750
IC1 318
TP10
R21 1K8
R23 1K5
C5 .047
+15V
R7 680
D1 BZY88-C5V1
PEDESTAL AMPLITUDE
28
500
25
31
R27 1K8
R28 3K9
R66 1K0
TR3 BCY70
R11 15K
R13 47K
TR4 BFW10
D3 1N914
C2 68p
R18 10K
C11 .047
D2 OA47
C30 270p
R15 1K8
R17 8K2
C29 22p
R16 1K8
IC2 318
R34 1K8
R36 1K5
TR1 BCY70
TR2 BSX20
D4 1N914
TR5 BFW10
INVERTED AREA GATE INPUT
32
R9 2K2
R10 1K5
R12 15K
C31 47p
R14 47K
-15V
R40 1K8
YCH INPUT
21
C3 100 (10V)
11
CHARACTER AMPLITUDE
5K0
10
9
R46 1K8
R47 4K7
C17 .047
R49 10K
7
CHARACTER SHIFT
10K
6
5
D5 1N914
C4 .033
R19 100
TR6 BCY70
R20 4K7
YOS INPUT
8
-15V
X INPUT (FROM X AMP CONTROL)
13
BEAM PROFILE INPUT
15

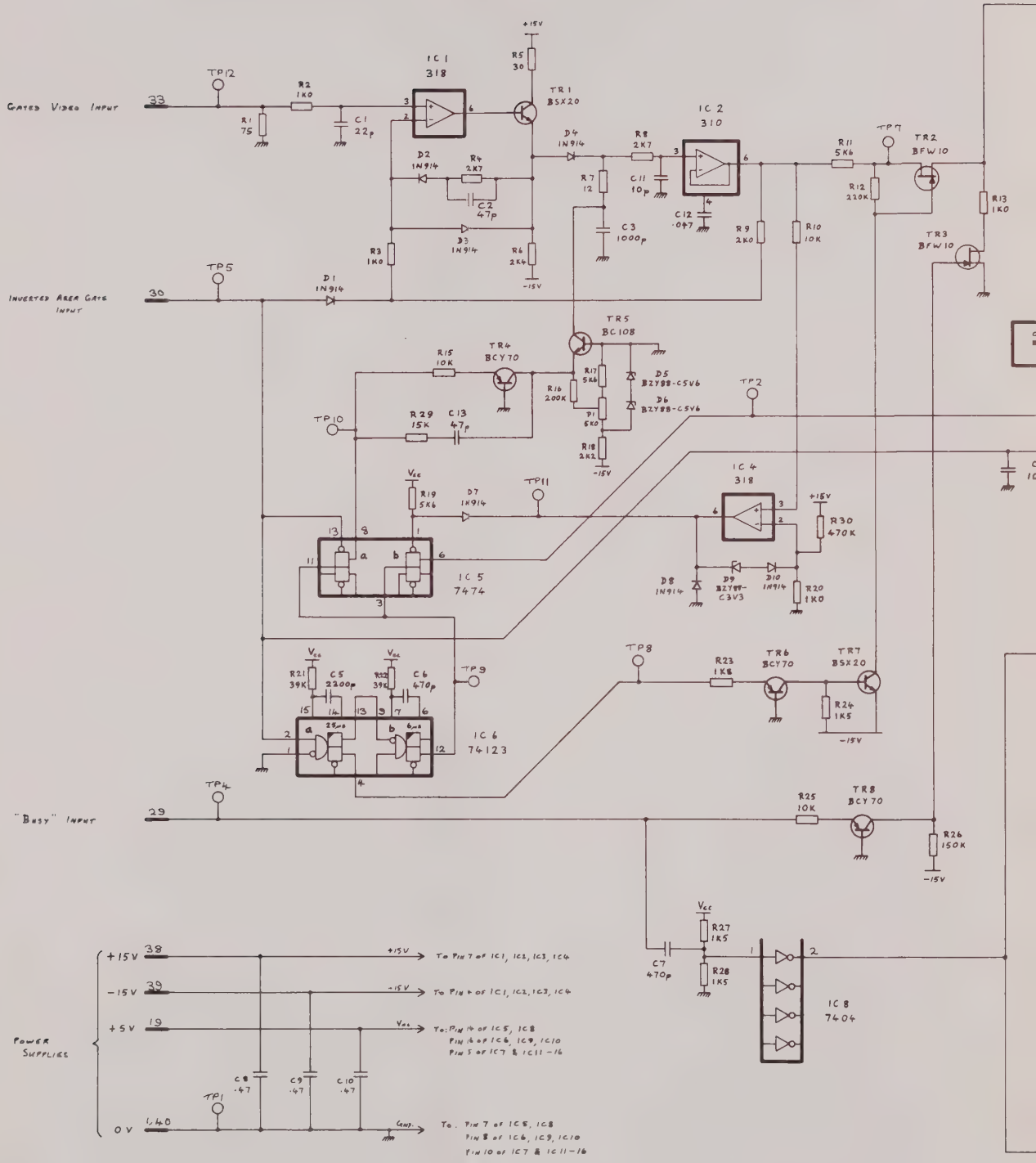


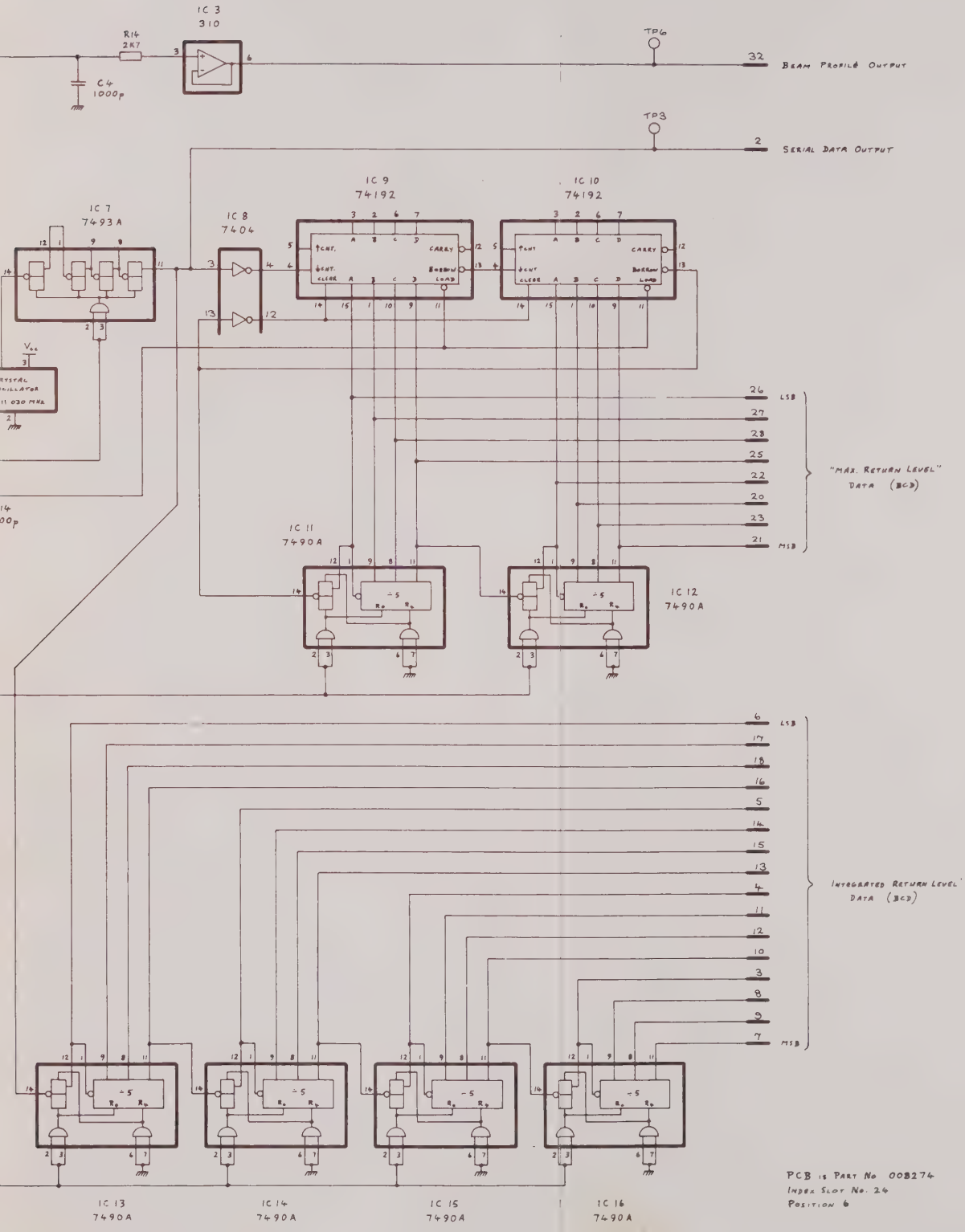
IC POWER SUPPLIES

IC TYPE	PIN NO	
	+15V	-15V
318	7	4
741	7	4
LH0002CH	1	7

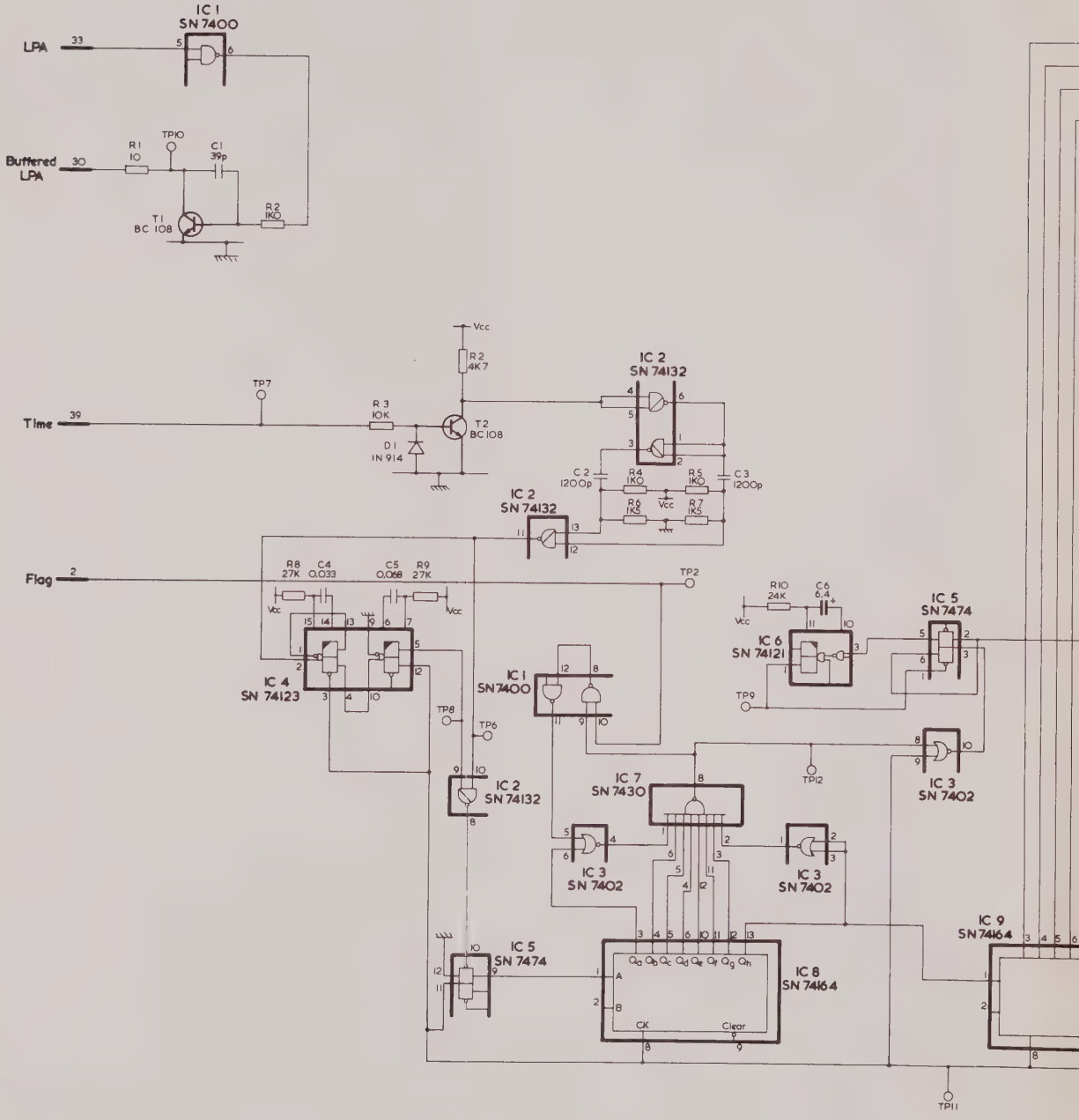
PCB IS PART NO. 008253
INDEX SLOT NO 26
POSITION 5

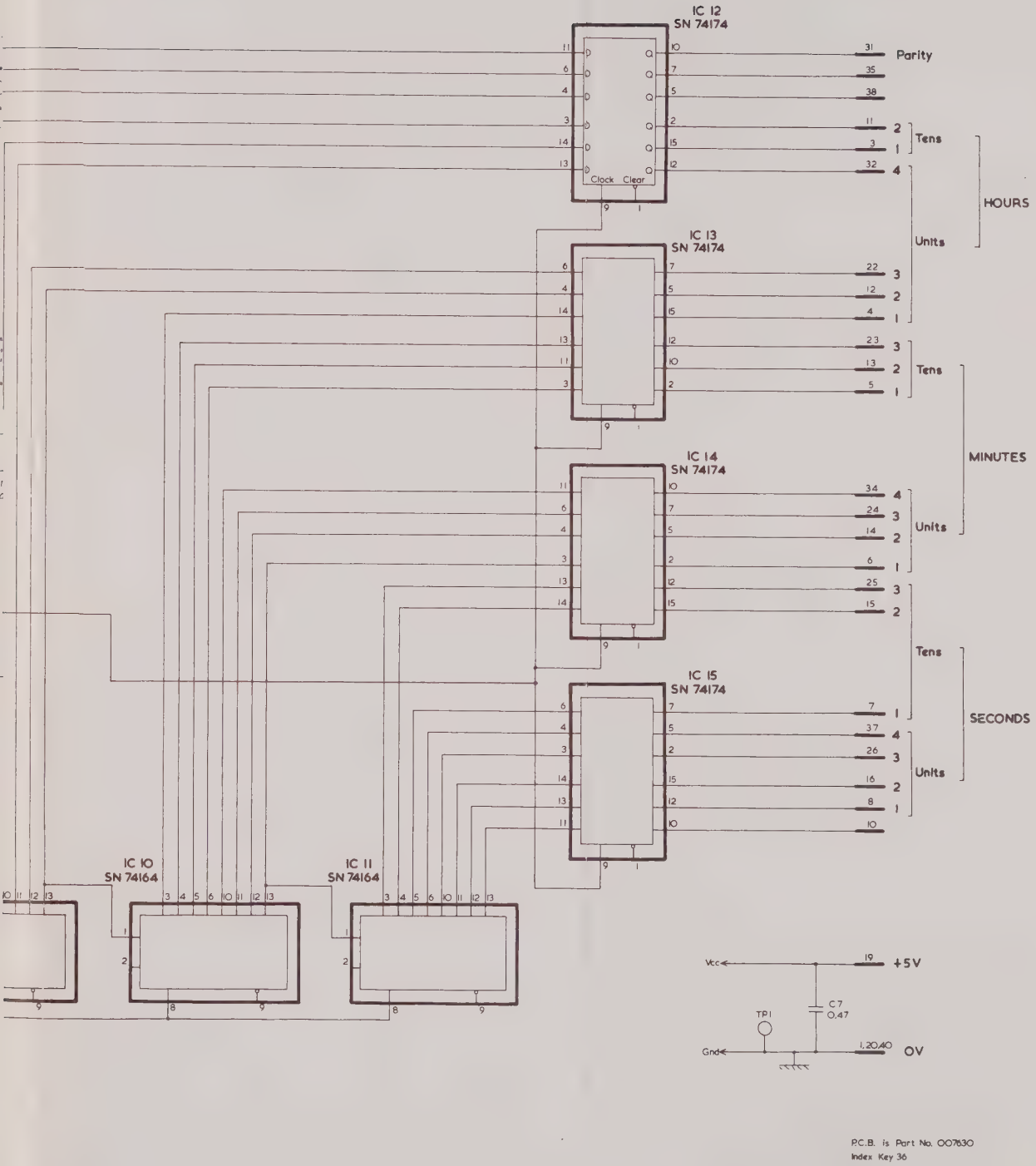
GSDA/1 – VIDEO ISOLATION BOARD


GATED VIDEO INPUT
33
TP12
R1 75
R2 1K0
C1 22p
IC 1 318
+15V
R5 30
TR1 BSX20
D2 1N914
R4 2K7
C2 47p
D3 1N914
R3 1K0
R6 2K4
-15V
D4 1N914
R8 2K7
C11 10p
C12 .047
C3 1000p
R7 12
IC 2 310
R9 2K0
R10 10K
R11 5K6
TP7
TR2 BFW10
R12 220K
R13 1K0
TR3 BFW10
INVERTED AREA GATE INPUT
30
TP5
D1 1N914
TR5 BC108
TR4 BCY70
R15 10K
R16 200K
R17 5K6
R18 2K2
P1 5K0
D5 BZY88-C5V6
D6 BZY88-C5V6
TP2
TP10
R29 15K
C13 47p
Vcc
R19 5K6
D7 1N914
TP11
IC 4 318
R30 470K
D8 1N914
D9 BZY88-C3V3
D10 1N914
R20 1K0
IC 5 7474
R21 39K
C5 2200p
R22 39K
C6 470p
TP9
IC 6 74123
TP8
R23 1K6
TR6 BCY70
TR7 BSX20
R24 1K5
"BUSY" INPUT
29
TP4
R25 10K
TR8 BCY70
R26 150K
C7 470p
R27 1K5
R28 1K5
IC 8 7404
POWER SUPPLIES
+15V
38
-15V
39
+5V
19
0V
1, 40
TP1
C8 .47
C9 .47
C10 .47
To Pin 7 of IC1, IC2, IC3, IC4
To Pin 4 of IC1, IC2, IC3, IC4
To: Pin 14 of IC5, IC8
Pin 16 of IC6, IC9, IC10
Pin 5 of IC7 & IC11-16
To. Pin 7 of IC5, IC8
Pin 8 of IC6, IC9, IC10
Pin 10 of IC7 & IC11-16



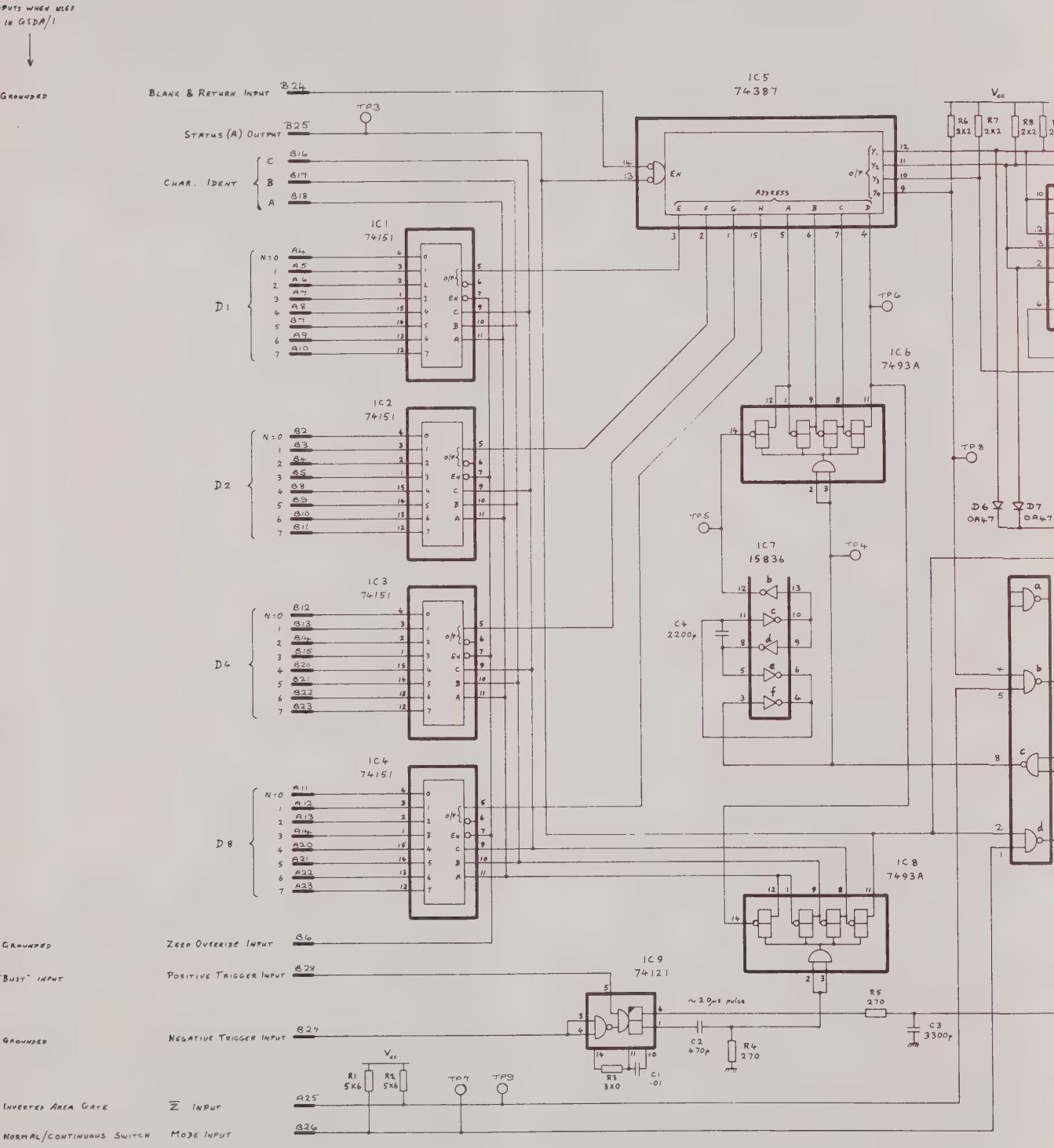
GSDA/1 – VIDEO MEASUREMENT BOARD CIRCUIT

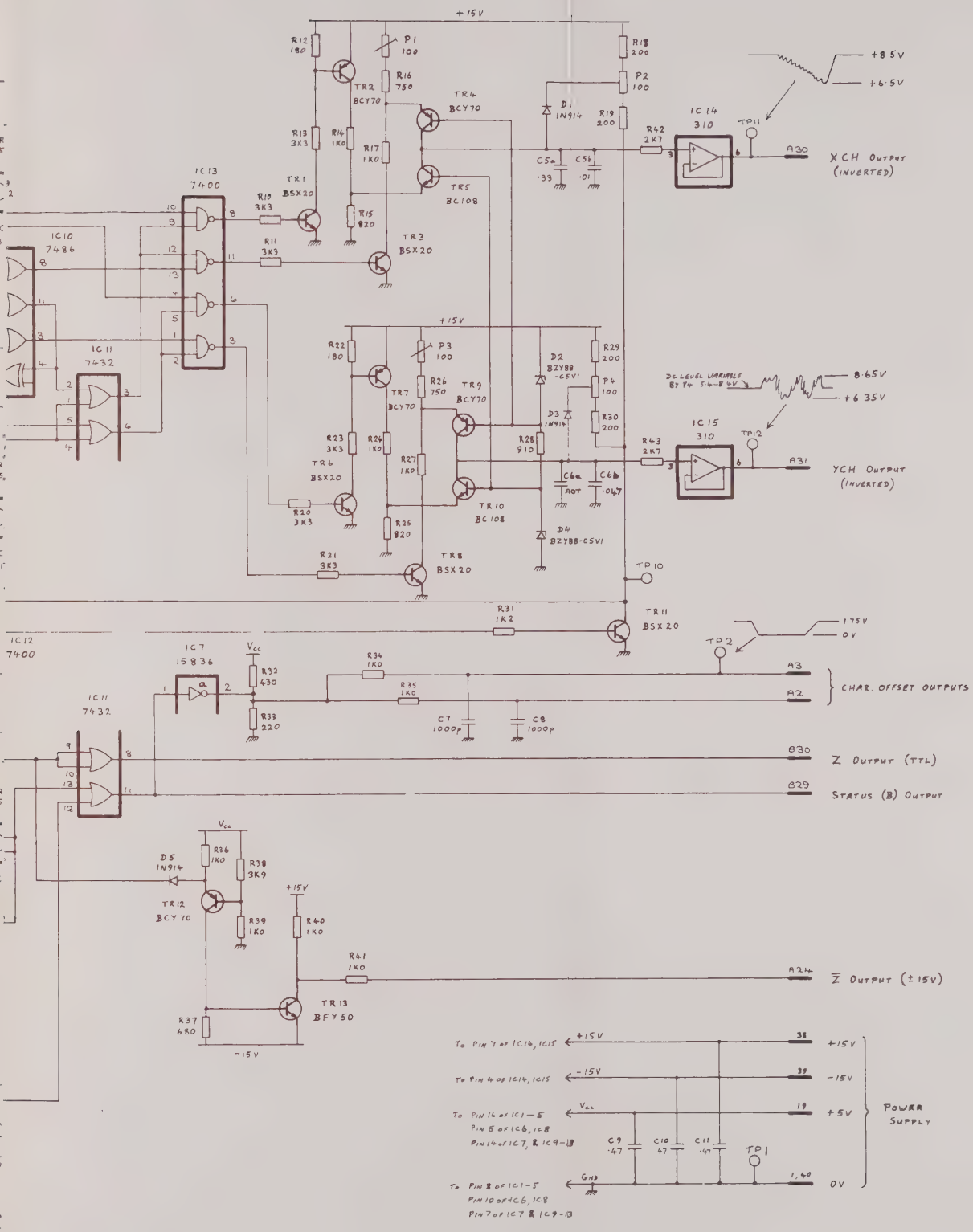

IC 1
SN 7400
LPA
33
TP10
R1
10
C1
39p
Buffered
LPA
30
T1
BC 108
R2
1K0
Vcc
R2
4K7
IC 2
SN 74132
TP7
Time
39
R3
10K
T2
BC108
D1
IN 914
C2
1200p
R4
1K0
R5
1K0
C3
1200p
R6
1K5
R7
1K5
IC 2
SN 74132
Flag
2
R8
27K
C4
0.033
C5
0.068
R9
27K
TP2
IC 4
SN 74123
IC 1
SN7400
TP8
TP6
IC 2
SN 74132
R10
24K
C6
6.4
IC 6
SN 74121
IC 5
SN 7474
TP9
TP12
IC 3
SN 7402
IC 7
SN 7430
IC 3
SN 7402
IC 3
SN 7402
IC 5
SN 7474
IC 8
SN 74164
CK
Clear
IC 9
SN 74164
TP11



P.C.B. is Part No. 007630
Index Key 36
Position 1

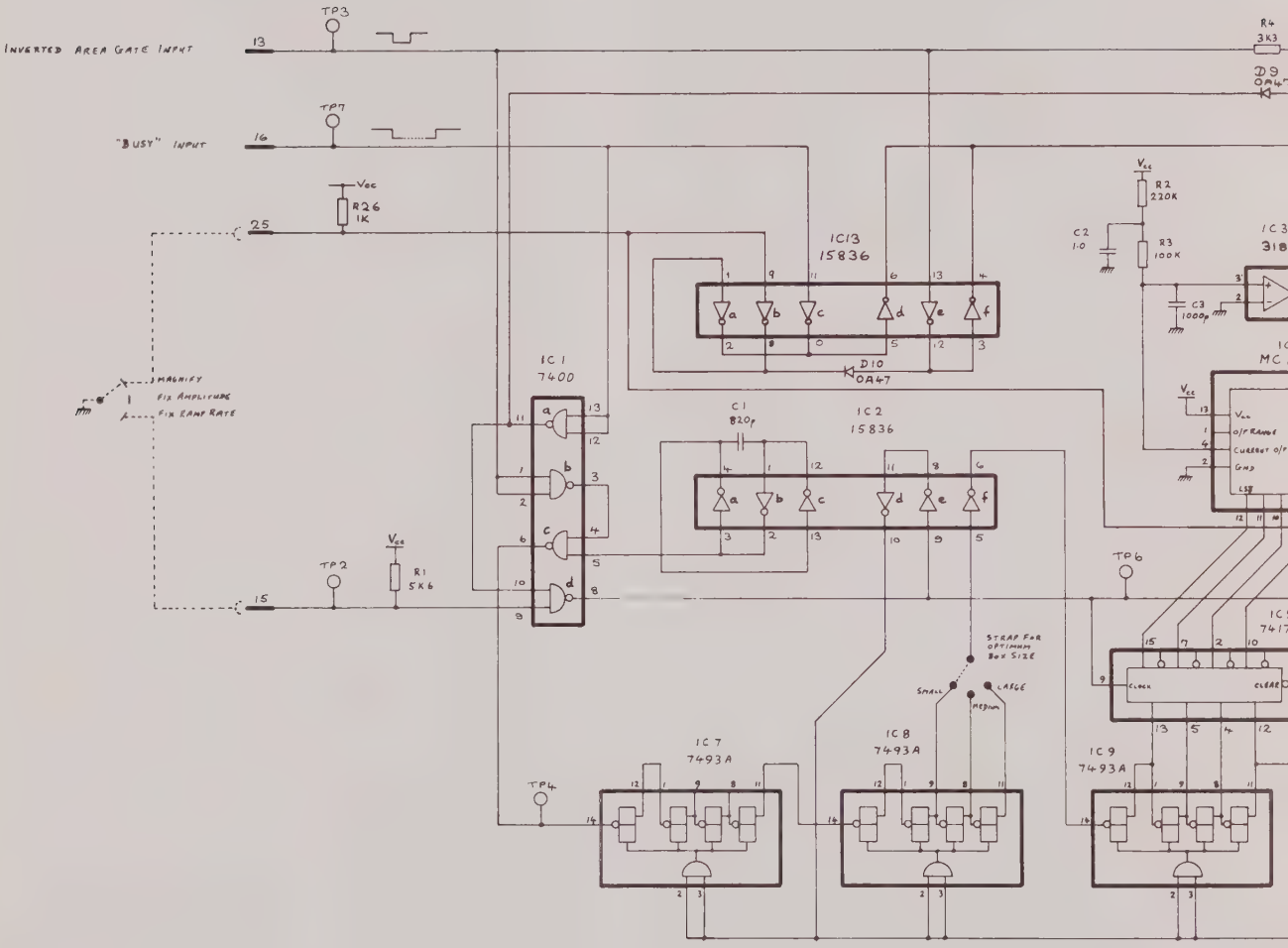
GSDA/1 – TIME DECODER CIRCUIT

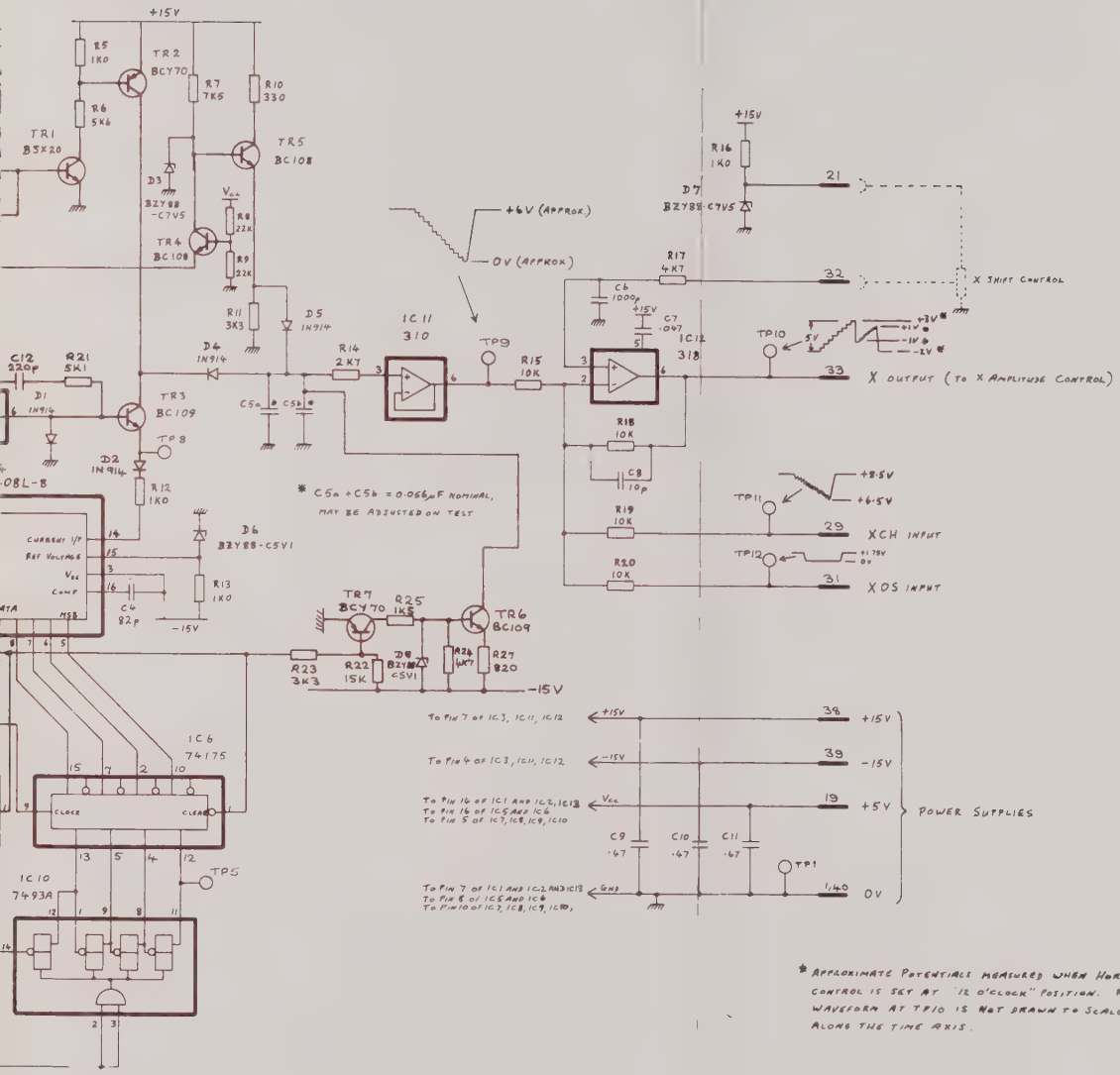

PUTS WHEN USED IN GSDA/1
GROUNDED
BLANK & RETURN INPUT
B24
STATUS (A) OUTPUT
B25
TP3
CHAR. IDENT
C
B
A
B16
B17
B18
IC5
74387
EN
ADDRESS
E F G H A B C D
Y0 Y1 Y2 Y3
O/P
Vcc
R6 2K2
R7 2K2
R8 2K2
IC1
74151
IC2
74151
IC3
74151
IC4
74151
D1
D2
D4
D8
N=0
TP6
IC6
7493A
TP8
D6 OA47
D7 OA47
TP5
TP4
IC7
15836
C4 2200p
IC8
7493A
GROUNDED
ZERO OVERRIDE INPUT
B6
"BUSY" INPUT
POSITIVE TRIGGER INPUT
B28
IC9
74121
~20ms pulse
R5 270
C3 3300p
C2 470p
R4 270
GROUNDED
NEGATIVE TRIGGER INPUT
B27
R3 3K0
C1 ·01
R1 5K6
R2 5K6
TP7
TP9
INVERTED AREA GATE
Z̄ INPUT
A25
NORMAL/CONTINUOUS SWITCH
MODE INPUT
B26



PCB is Part No. 008246
Index Slot No 32
Position 2

GSDA/1 – CHARACTER GENERATOR


INVERTED AREA GATE INPUT
"BUSY" INPUT
TP3
TP7
TP2
TP4
TP6
13
16
25
15
Vcc
R26
1K
R1
5K6
R2
220K
R3
100K
R4
3K3
C1
820p
C2
1·0
C3
1000p
D9
OA47
D10
OA47
IC1
7400
IC2
15836
IC13
15836
IC3
318
IC7
7493A
IC8
7493A
IC9
7493A
MAGNIFY
FIX AMPLITUDE
FIX RAMP RATE
STRAP FOR OPTIMUM BOX SIZE
SMALL
MEDIUM
LARGE
CLOCK
CLEAR



* APPROXIMATE POTENTIALS MEASURED WHEN HORIZONTAL SHIFT CONTROL IS SET AT "12 O'CLOCK" POSITION. NOTE THAT THE WAVEFORM AT TP10 IS NOT DRAWN TO SCALE, PARTICULARLY ALONG THE TIME AXIS.

PCB IS PART NO 008232

INDEX SLOT NO 30

POSITION 3

GSDA/1 – INTERRUPTED RAMP GENERATOR

INSTRUCTION CODES

Instruction	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	
Marker Y	X	X	X	X	0	0	0	1	
Send Data N	N_1	N_2	N_4	N_8	0	0	1	1	
Marker Z	X	X	X	X	0	1	0	1	
Conditional Jump to A (A_1 remains unchanged)	A_{16}	A_8	A_4	A_2	0	1	1	1	
End (set flag low)	X	X	X	X	1	0	0	1	
L2 In: Send space and set Zero Suppression L2 Out: Send space and extend print Set	0	0	0	0	1	0	1	1	Also see note on L2 below.
L2 In: Clear Zero Suppression L2 Out: Restore normal print.	X	X	X	X	1	1	0	1	
Jump to A = 0 (reset)	X	X	X	X	1	1	1	1	
Send Character T	$\overline{T_1}$	$\overline{T_2}$	$\overline{T_3}$	$\overline{T_4}$	$\overline{T_5}$	$\overline{T_6}$	$\overline{T_7}$	0	

NOMENCLATURE

Group Symbol	Bit Symbols	Remarks
A	$A_{16}, A_8, A_4, A_2, A_1$	Instruction No
B	$B_0, B_1, B_2 \ldots\ldots B_7$	Instruction Code
D	D_1, D_2, D_4, D_8	BCD Data
N	N_1, N_2, N_4, N_8	Data Source Address
T	$T_1, T_2, T_3 \ldots\ldots T_8$	ASCII Character

CONTROL INPUTS

Note that Application of Logic 1 or open circuit to any input has no effect

Application of Logic 0 to an input has the following effects:

Blank: "Send Data" instruction causes a space character to be sent instead

Repeat: Causes continuous repetition of next instruction

Reset: Causes immediate jump to instruction 0, and stops program if optional link is fitted. Note that instruction 0 will not be executed unless Repeat input is held low until execution commences

Jump Enable: Causes conditional Jump instruction to be ignored. Program continues to next instruction

Begin: Negative-going edge sets flag high. Program continues to next instruction

ASCII Input: (Ignored when flag is high) But appears at output when flag is low

Interrupt: Causes program to stop after execution of current instruction

OUTPUTS

Flag: High = Busy; Low = Stopped. Flag can only be set low by programmed instruction unless link from Reset input is fitted

ASCII: Output code in true ASCII, with either odd or even parity bit may be generated on board or (if flag is low) from external source

Tone: 1 kHz (nominal) carrier, amplitude-modulated by ASCII output above. Note that "tone" = mark, "no tone" = space

Marker Y and Marker Z: 2 μs pulse to low level when appropriate "Marker" instruction in program is reached

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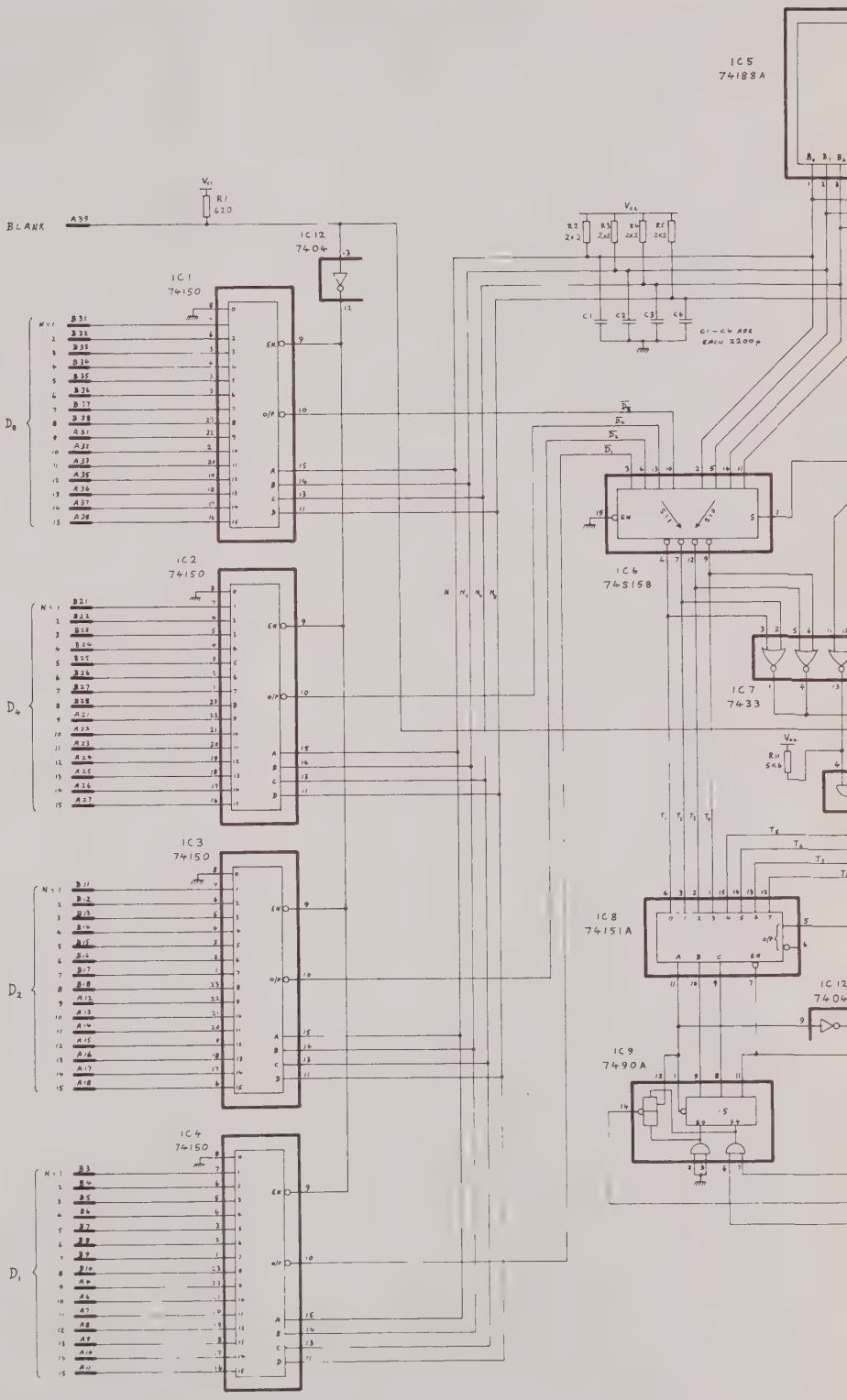
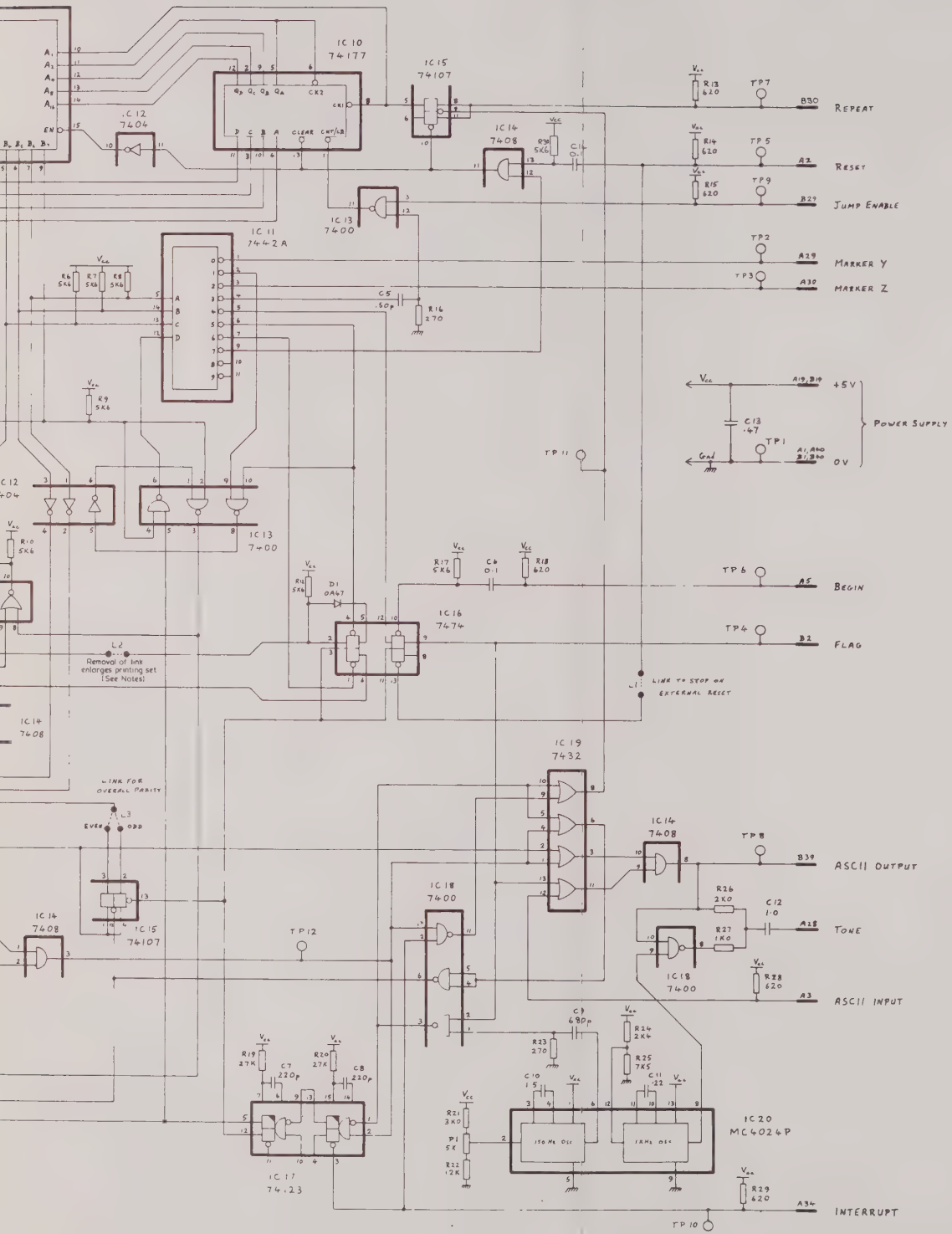
L2: Referring to the Programming Guide (D 499901)

BCD coded data normally (ie L2 in) causes a character to be printed from column 4 of the coding table, eg. BCD 2 causes a number two or BCD 13 causes an equals sign.

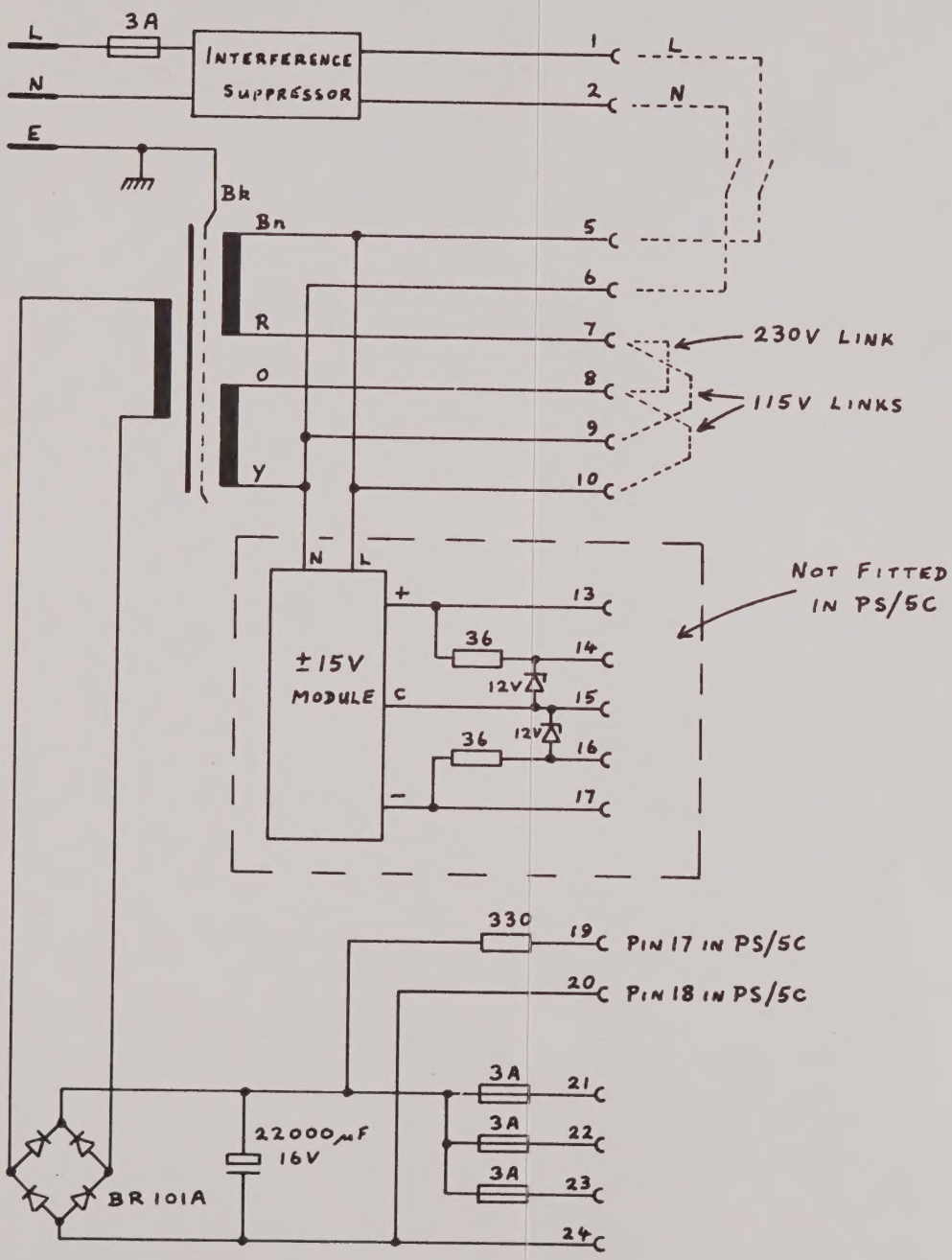
If L2 is removed and the Extend Print Set command is given, subsequent BCD coded data will cause characters from column 5 to be printed, eg BCD 2 would give inverted commas or BCD 13 would give a minus sign





PCB is Part No 007602
Index Key 20
Position 2

GSDA/1 — FORMATTER CIRCUIT



GSDA/1 – PS/5C POWER SUPPLY UNIT

MP MASTER
MA23844